BGA 1 & 2

COURSE NOTES

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Telecom Australia
Engineering Training Section
Services Branch - N.S.W.

B.G.A. 1 and 2 Course Notes

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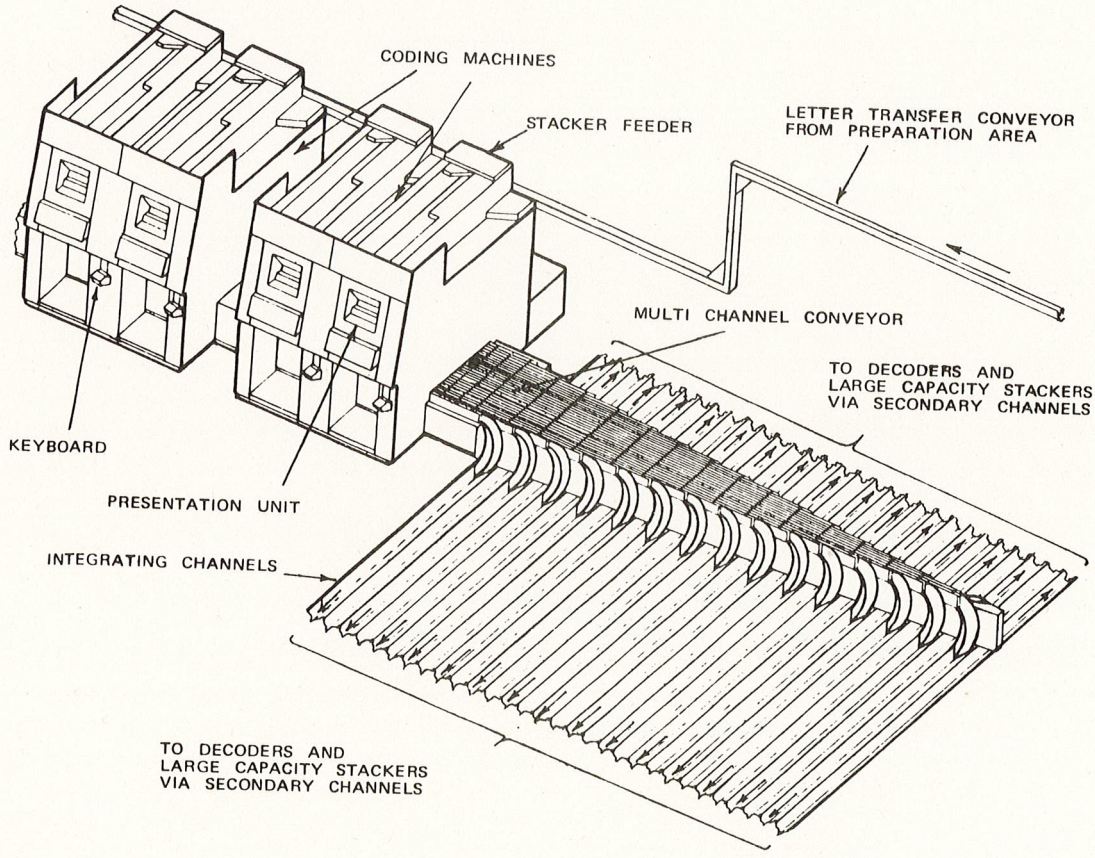
Section 1

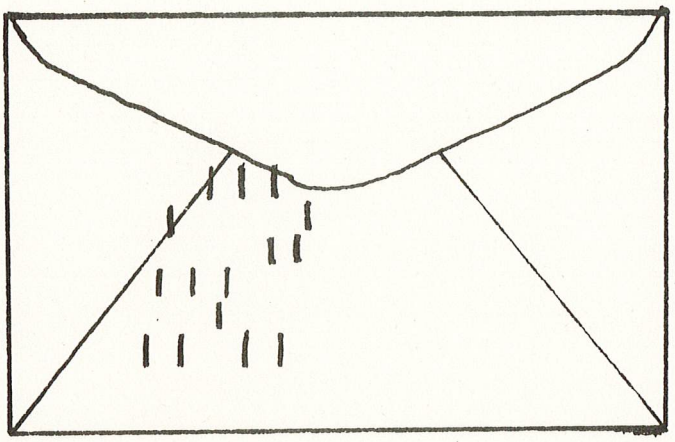
Logic Based Systems

(a) Mail Handling System

This system uses a basic processor to provide sorting information, dependent upon information fed in. The operator feeds in address information via a key board to the register translator. The register translator then returns information regarding the sorting operations required to the coding machine where some information is used to control the primary sort (operations within the coder to send the letter to a broad classification e.g. Country City etc) whilst other information is used to place the secondary sorting information on the rear of the envelope in binary code.



CODING MACHINE SUITE (PART).



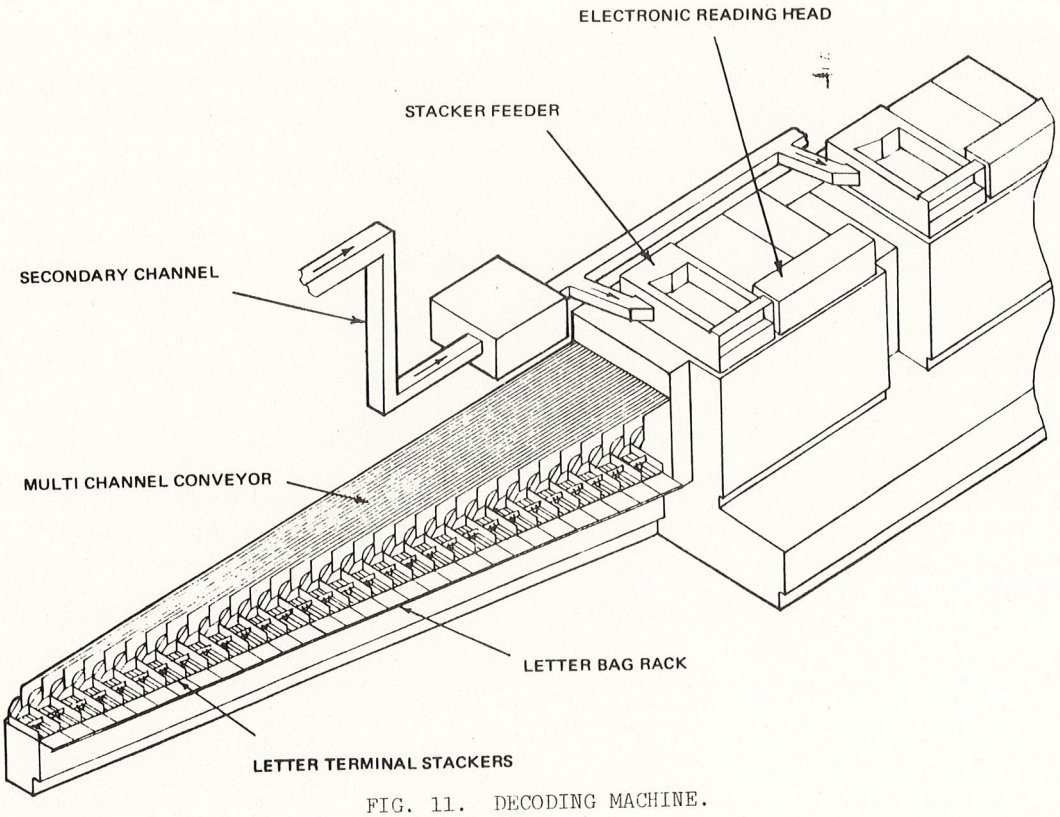
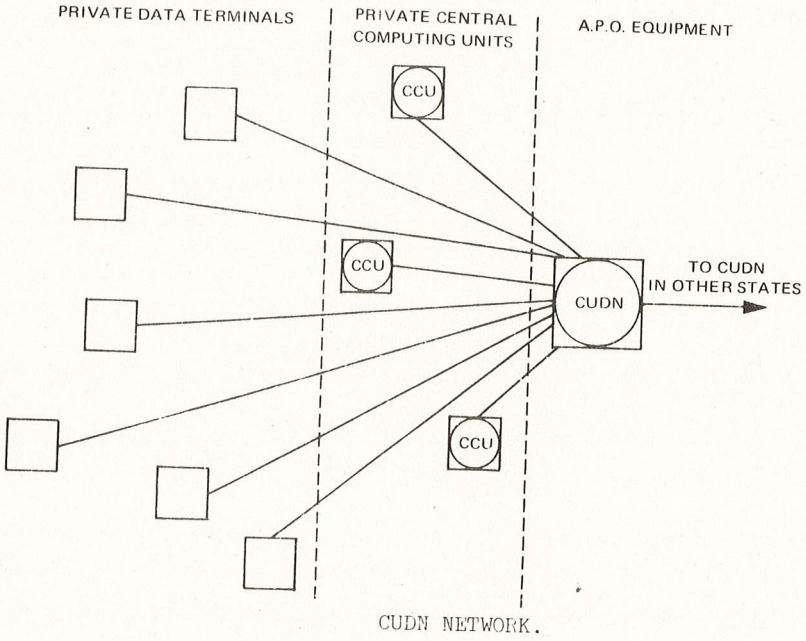


FIG. 11. DECODING MACHINE.

(b) C.U.D.N. - Telnet

C.U.D.N. (Common User Data Network)

Originally designed to connect private terminals to main computer via switching network. The C.U.D.N. is a computer controlled data switching network which provides a customer with the facilities of a private store and forward network with shared network economy.



The store and forward principle allows for the transmission of data to the C.U.D.N. before a path to the destination is established. By sharing the network with other organisations a considerable saving is achieved in the provision of equipment and trunks. Compatibility is only required between the C.U.D.N. and the terminals, and provides entry and exit points throughout the Commonwealth via centres located in each state.

The C.U.D.N. does not engage in general data processing but provides only communication for a customers data. Because the C.U.D.N. did not receive sufficient support from the private sector and the fact that small computers became popular, the C.U.D.N. computer is now unsuitable for the needs of the private sector. The commission changed the function of the C.U.D.N. to that of TELNET.

TELNET (Telecom Network)

This system uses the C.U.D.N. computer with a similar programme. It is a computer controlled data switching network as for C.U.D.N., so that its basic function is unchanged. The major difference is that all terminals connected to the network are Telecom controlled (e.g. Exchanges SDC's, SID's, etc).

TELNET SYSTEM OPERATION

When a customer does business with Telecom a form is filled out in the usual way. The operator at a business office will then decide what type of form is required e.g. New Service
Removal
In situ service etc.,

Each of these forms has a particular code and this is entered via the V.D.U.

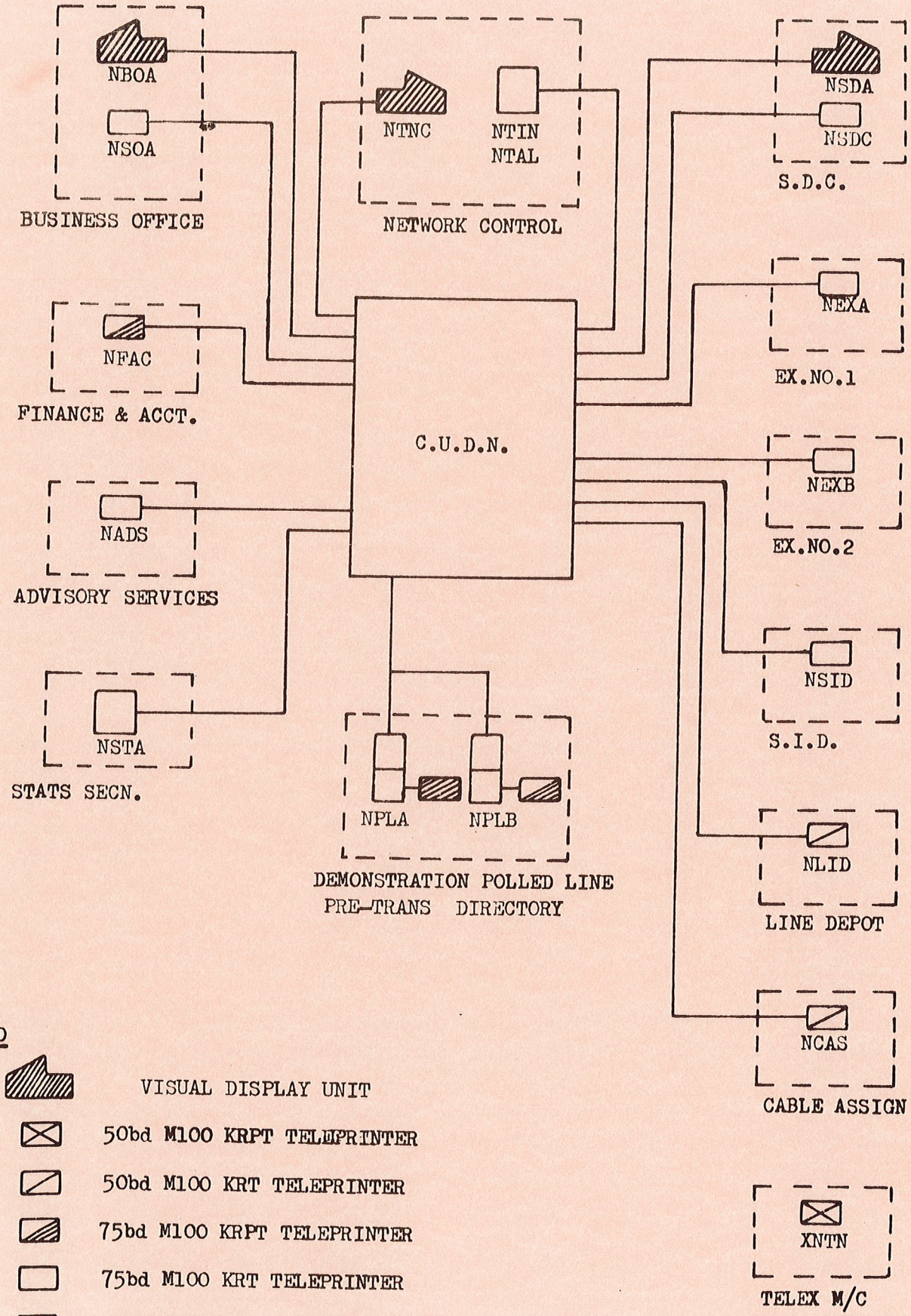
The C.U.D.N. computer then receives this code and causes the appropriate form to be displayed on the V.D.U. screen. All form formats are stored within the computers memory.

The operator then proceeds to fill in the form on the V.D.U. screen according to the information supplied by the customer. When satisfied that the information on the screen corresponds to what is required, the operator then causes the V.D.U. to send the completed form to the C.U.D.N. computer at 4800 BPS.

The computer receives the information and then according to the address proceeds to send the information to a number of locations e.g. SID, Exchange, Line Depot. These locations may use any one of the various telegraph machines in current use and speeds vary from 50 BAUD machines to 300 BAUD machines. The computer decides speed and format at which to send out the information.

The information will be received at these locations as a print out on the teleprinter but in the same format as the present telephone order form and when work is completed a completion order can be sent back ove r the same network.

This system will eventually allow the commission to do away with a lot of telephone order processing. For example under the present system when a customer completes the application form up to 15 copies of the telephone order have to be prepared and despatched to various locations. Under TELNET the only processing to be done is the input operation at a V.D.U. or similar device, and the actual completion of the telephone order by those directly concerned. The diagram below sets out the connections that are required. The system shown is the system installed in Haymarket Exchange to test out the system but the principle has been applied in the Parramatta Area as a trial.



LEGEND

- VISUAL DISPLAY UNIT
- 50bd M100 KRPT TELEPRINTER
- 50bd M100 KRT TELEPRINTER
- 75bd M100 KRPT TELEPRINTER
- 75bd M100 KRT TELEPRINTER
- 75bd M100 RO TELEPRINTER
- T/108 AND SCU
- TERMINET 300 DATAPRINTER

The TELNET System using the C.U.D.N. Computer is maintained and operated solely by Technicians, T.T.O.'s and S.T.O.'s as opposed to other computer areas which are operated by Telecom personnel but maintenance is provided by persons outside the Commission.

A.D.P. - Automatic Data Processing

This installation is installed at West Street, North Sydney and comes under the control of Information Systems branch. The system is operated by Telecom personnel (e.g. Computer Operators and Programmers) but maintained by the manufacturers personnel Honeywell Corporation.

The installation is used to process telephone account information and compiling and printing telephone accounts to the point of placing them in envelopes ready for despatch.

This installation, which has three computer systems housed in the same building can also be used for general data processing such as statistical records, ADR records and reports and also has research capabilities.

Two of the three systems are magnetic tape as their main bulk storage medium with some magnetic disc used. The third system is a more modern computer of 3rd generation construction which uses magnetic disc storage as its main medium. All three systems make extensive use of high speed printerswhich are described later in this note.

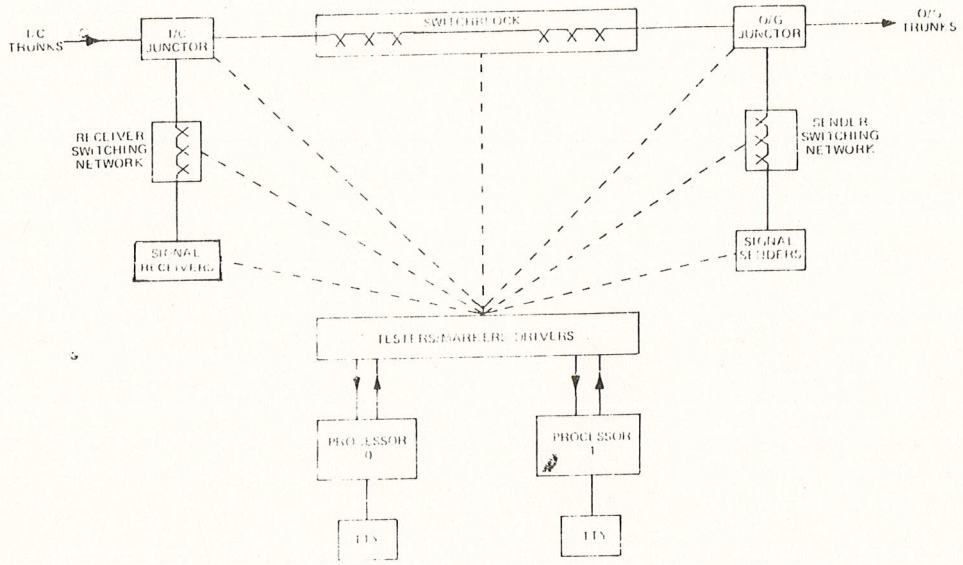
Stored Programme Control Exchange 10C Exchange Pitt Street, Sydney.

This exchange is a computer controlled switching network dealing exclusively with trunk traffic e.g. S.T.D., I.S.D., Operator Connected cables.

The system bears some resemblance to ARF Crossbar in that it is a common control exchange but instead of markers, registers etc., to do the controlling a computer or processor does the job. In this system three processors are used for security.

The processors controlling calls in the exchange work in what is termed real time mode meaning they handle calls as they occur,as opposed to general purpose computers which provide results some time after the information is fed in. The processors work in times of nano secondsand voltages of 5V and OV, therefore interfaces are required to act as buffer for speed and voltage levels.

The interfaces used are shown on the diagram below and consist of testers, markers and drivers. The switch block consists of switching matrix made up of reed relays.



TYPICAL EXCHANGE.

Testers - act as scanning device constantly checking the condition of all devices controlling the switch block. Any information determined in this way is passed on to the processor for action.

Markers - control the operation of the various devices and act as the time interface for the system. These are slow speed storage devices e.g. relays.

Drivers - act on the power interface in that they increase or decrease the voltage levels as required (e.g. from processor to exchange from +5/0V to 48 V & eth).

Functions of other parts are as follows:-

Junctors provide the interface between junctions and the exchange in much the same way as the line circuit in normal exchanges. One junctor is provided per line. They are also required to send and receive line signals whether MFC or decadic and hold the call once it is set up.

Signal Senders and Receivers are provided on a shared basis and or, connected to the junctors via send/receive switching network. Two categories are provided MFC and Decadic.

ARE 11

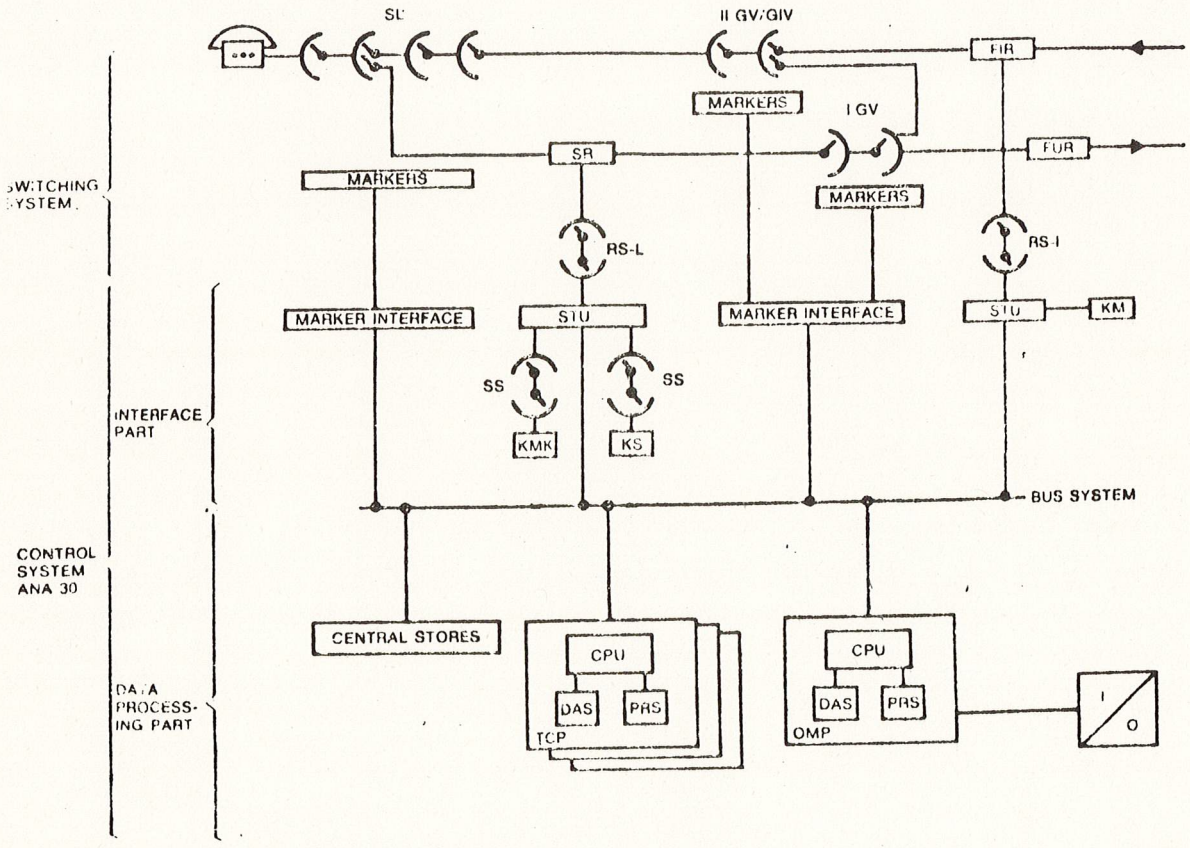
ARE 11 system consists of an ARF crossbar switching system (modified) and an ANA30 electronic register processor. The system can be installed as a completely new exchange or as a modification to an existing system.

General

ANA 30 system replaces relay type registers with a new simplified register which uses minature relays and electronic circuitry mounted on printed circuit cords which are mounted in plug in shelves or modified ARF racks. This simplified register has a name change and now becomes a S.T.U. (Signal Transfer Unit).

The analysis functions previously performed by the relay type markers and registers are now performed by the ANA30 equipment (specifically in the Traffic Control Processor in conjunction with the stores). These functions are controlled by the stored programmes in the T.C.P.

Communication between the technical staff and the system is by means of input/output units either Teleprinters V.D.U.'s or tape readers. These devices are connected via suitable interfaces to the O.M.P. (Operations and Maintenance Processor).



SIMPLIFIED TRUNKING DIAGRAM - ARE 11 EXCHANGE.

SECTION 2

NUMBER SYSTEMS

This section details the various types of number systems used in computer controlled equipment.

Accepted convention is the decimal or "base 10" system where the digits 0 - 9 are used.

i.e. 0 1 2 3 4 5 6 7 8 9

When highest digit (9) is reached a 1 is placed in the next column and written as 10 or (ten).

Therefore in this system 978 is:-

9 hundreds - 9×10^2

7 tens - 7×10^1

8 units - 8×10^0

This system is unsuitable for use in mechanical or electrical counting.

The system used within computers and other logic devices is the Binary or Base 2 system, where only two figures are used. 0 x 1

These two conditions may be represented by a switch ON or OFF.

A relay contact closed or open

A current or no current in a circuit

A change of polarity on a circuit etc.

The Binary scale is obtained in the same way as decimal with one minor change.

i.e. Numbers are expressed as powers of 2 and not powers of 10

Decimal Notation	Powers of Two	Numbers of Various Powers					Binary Notation
		2^4 16 zone	2^3 8 zone	2^2 4 zone	2^1 2 zone	2^0 1 zone	
0		.	.	.	.	.	0
1	2^0	.	.	.	.	1	1
2	2^1	.	.	.	1	0	10
3	$2^1 + 2^0$	.	.	.	1	1	11
4	2^2	.	.	1	0	0	100
5	$2^2 + 2^0$	.	.	1	0	1	101
6	$2^2 + 2^1$	.	.	1	1	0	110
7	$2^2 + 2^1 + 2^0$	.	.	1	1	1	111
8	2^3	.	1	0	0	0	1000
9	$2^3 + 2^0$	.	1	0	0	1	1001
10	$2^3 + 2^1$	.	1	0	1	0	1010
11	$2^3 + 2^1 + 2^0$	.	1	0	1	1	1011
12	$2^3 + 2^2$	.	1	1	0	0	1100
13	$2^3 + 2^2 + 2^0$	.	1	1	0	1	1101
14	$2^3 + 2^2 + 2^1$	.	1	1	1	0	1110
15	$2^3 + 2^2 + 2^1 + 2^0$	.	1	1	1	1	1111
16	2^4	1	0	0	0	0	10000

One method of converting Decimal numbers into binary would be to find the zone number whose sum is the number required.

Allot a 1 for each zone used and a 0 for each unused zone.

Example

24 as Binary Number

16 + 8 are zones used

1, 2, 4 are unused

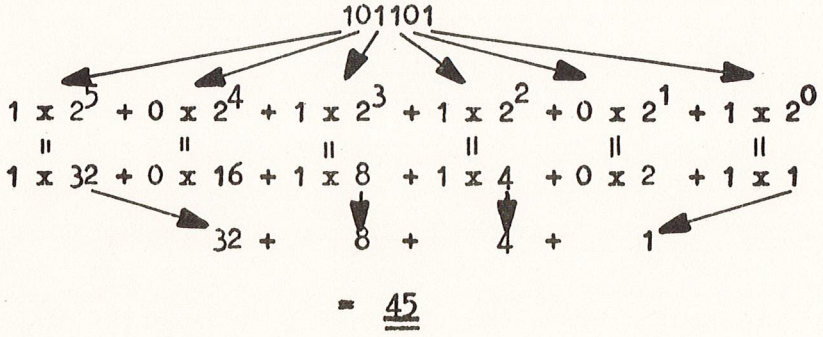
∴ Number 24 in Binary is 11000

Simple method of converting decimal to binary. Merely divide by 2 repeatedly until the result is zero. Writing the remainders as they occur.

2 / 24		
2 / 12	0	LSB
2 / 6	0	Written 11000
2 / 3	0	
2 / 1	1	
0	1	MSB

To convert a binary number to decimal simply add the weighting applied to each bit.

Example



= 45

Binary Addition

There are 55 combinations to be memorised to perform addition in the decimal system to the binary system only 3 combinations need be memorised.

+	0	1	2	3	4	5	6	7	8	9
0	0	1	2	3	4	5	6	7	8	9
1	1	2	3	4	5	6	7	8	9	10
2	2	3	4	5	6	7	8	9	10	11
3	3	4	5	6	7	8	9	10	11	12
4	4	5	6	7	8	9	10	11	12	13
5	5	6	7	8	9	10	11	12	13	14
6	6	7	8	9	10	11	12	13	14	15
7	7	8	9	10	11	12	13	14	15	16
8	8	9	10	11	12	13	14	15	16	17
9	9	10	11	12	13	14	15	16	17	18

+	0	1
0	0	1
1	1	10

TABLE 3

As can be seen from the Table 3 only 1 combination has a carry.

Examples of Binary Addition

100	1001	110	1010	1100110
+ 011	+ 0101	+ 011	+ 0111	+ 1010011
111	1110	1001	10001	10111001

Binary Subtraction

When binary digits are subtracted from one another only one combination involves borrowing as shown in the table below. The digit carried is subtracted in the next column to complete the subtraction operation.

Example

110	10011
- 101	- 1000
001	01011

-	0	1
0	0	1
1	b1	0

b shows borrowing operation involved.

This process of subtraction can be accomplished outisde a machine by human minds, but within a machine the subtraction operation can be done by taking the complement of the number to be subtracted and adding the two numbers together. This is called 2^s complement operation.

The complement of a number is that number, which, when added to the original,

(i) Completes the highest number that can be contained in the columns used in the number

or

(ii) Completes the number to the next power of the base. This number is always 1 more than case (i)

E.G. In the decimal or base 10 system case (i) is called the nine's complement and in binary it is called the one's complement.

Case (ii) is called the ten's complement in decimal and in binary it is called the two's complement.

In practice the ten's or two's complement is meant when the word complement is used on its own.

E.G. The complement of 21 is 79

$$\begin{array}{r} 21 \\ +\ 79 \\ \hline 100 \end{array}$$

What is the complement of 6, 14, 36, 134, 3642? (Base 10)

The 1's complement of a binary number is each bit of the number inverted. This is readily available in a machine.

E.G. The 1's complement of 1011 is 0100

E.G. The 2's complement of 10101 is 01011

$$\begin{array}{r} 10101 \\ +\ 01011 \\ \hline 100000 \end{array}$$

To obtain the 2's complement of a binary number - invert each bit and add 1 to the least significant bit.

E.G.

	10101	
Inverted	01010	(one's complement)
add 00001	00001	
	01011	two's complement

The sign bit. Machines cannot understand + and - signs so binary numbers must be used in their place. 0 represents +ve numbers

1 represents -ve numbers

is the usual representation and they are written in the most significant column.

E.G. $(6.25 - 4.25)_{10}$ OR $((0)\ 110.01 - (0)\ 100.01)_2$

Subtraction using the signed 2's complement

$+ 6.25_{10}$	=	$(0)\ 110.01_2$	Minuend
$- 4.25_{10}$	= -	$(0)\ 100.01_2$	Subtrahend

The 2's complement of the subtrahend is added to the minuend. If the sign bit of the sum is 0 the result is the true difference and is positive (+ve). If the sign bit is 1 the result is the 2's complement of the difference. Try overflow is lost.

	(0) 110.01	
add	(1) 011.11	2's complement of (0) 100.01
	$_1$(0) 010.00	= 2 (+ve)
	Lost	

Add two negative numbers

-5 + (-7)

Assuming a word length of 5 bits, all unused or insignificant bits will be 0.

+5 = binary (0) 0101

-5 in 2's complement form

= (1) 1011

+7 = binary (0) 0111

-7 in 2's complement form

= (1) 1001

-5	=	(1) 1011
-7	=	(1) 1001
		$_1$(1) 0100
		Lost

The result is the 2's complement of the correct answer which is negative. Indicate by (1).

= - (0) 1100 = -12_{10}

1011
ADD 1
1100

Subtraction by signed 1's complement

The 1's complement of the subtrahend is added to the minuend and the overflow bit (not the sign bit) is added to the least significant bit of the uncorrected sum.

If the sign bit of the correct sum is 0 then the result is the true difference and the number is positive. If the sign bit is 1 then the result is the 1's complement of the difference and the number is negative.

E.G. 9.5 - 5.25

or (0) 1001.10 - (0) 0101.01 in binary

The 1's complement of (0) 0101.01

is (1) 1010.10

thus 9.5 = (0) 1001.10
- 5.25 = (1) 1010.10 } ADD.

adding 1(0) 0100.00

→ 1 end-around-carry

(0) 0100.01 corrected sum

difference = (0) 0100.01 or 4.25_{10}

Octal Number System

Base 8 system.

Where a binary weighting was shown as

2^3 2^2 2^1 2^0

and in decimal

10^3 10^2 10^1 10^0

In Octal the weighting becomes

8^3 8^2 8^1 8^0

In the base 8 system only the digits 0 - 7 are used.

To convert decimal to octal simply divide by 8 until the result is zero, the remainder becomes the octal result.

Example

26_{10} to Octal

8 / 26	2
8 / 3	3
0	

$26_{10} = 32_8$

93_{10} to Octal

8 / 93	
8 / 11	5
8 / 1	3
0	1

$93_{10} = 135_8$

To convert Octal to decimal.

Example 72_8 can be written as:-

$$= 7 \times 8^1 + 2 \times 8^0$$
$$= 7 \times 8 + 2 \times 1$$
$$= 56 + 2$$
$$= 58_{10}$$

Check by converting 58_{10} to Octal

$8 \overline{)58}$ 2

$8 \overline{)7}$ 7

0

$= 72_8$

To convert Octal to binary is easily done by writing a 3 digit binary number for each Octal digit.

Example 72_8

111 010 111010

The Octal number system is used for easy direct input/output operator because it is simply converted to binary and vice versa.

Hexidecimal Number System

As binary numbers become very long the hexidecimal system is often used as a abbreviated form of writing to reduce the chance of error. Digits 0 - 9 and A - F are used to represent decimals 0 - 15.

CONVERSION TABLE		
DECIMAL (10)	BINARY (2)	HEXADECIMAL (16)
0	0	0
1	1	1
2	10	2
3	11	3
4	100	4
5	101	5
6	110	6
7	111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F.

To convert longer binary numbers to Hex. Divide the binary number into groups of 4 from the right.

Example

0111	1101	0111
7	D	7

$7D7_{16}$

Conversion of Decimal to Hexidecimal. Divide by 16 and note remainder until result is zero. Then convert any remainder between 10 and 15 to its Hexidecimal Equivalent A - F.

Example

16 / 193 = 12

16 / 12 12 = C

0

193 = C1

Hexidecimal allows binary numbers to be easily read. For example in the data store with the C.P.U. of the ARE II system there are 128 Words each of 8 Bits. If the contents of this store were printed out in binary form errors could be possible. The print out provided is in Hexidecimal as shown below and the operating staff would then use a conversion chart to extract relevant information.

teleprinter read out in hexadecimal code. A conversion chart would be used by operating staff to interpret the information in the table.

00	02														
03	06	03	06	13	40	00	00	01	02	20	00	18	00	16	0A
54	25	0C	15	00	0B	00	00	00	00	00	A3	70	0F	0F	00
04	0C	00	00	E6	00	20	11	FF	20	21	FF	20	09	3C	10
18	01	12	41	00	00	00	01	00	01	B0	14	30	11	78	00
00	0B	01	B0	0B	10	4B	8D	00	00	00	00	14	F5	08	85
00	85	00	04	90	01	04	02	02	CB	05	27	72	00	42	16
20	11	03	06	A0	80	00	00	00	20	00	00	00	00	00	00
3E	05	3E	02	00	00	00	00	00	00	00	00	00	00	60	0D;

HEXADECIMAL READ OUT.

Adding Hexidecimal Nos.

Examples

21A	72C	207A
+ 352	A3F	8194
56C	116B	A21E

SECTION 3

CODES

BCD Code - Binary Coded Decimal

This code is a variation of the binary number system. Each decimal number from 0 - 9 is coded using a 4 Bit Binary Code. See examples below:-

COLUMN VALUE	8	4	2	1	
	0	0	0	0	BCD = DECIMAL 0
	0	0	0	1	BCD = DECIMAL 1
	0	0	1	0	BCD = DECIMAL 2
	0	0	1	1	BCD = DECIMAL 3 (Column 1 + 2)
	0	1	0	0	BCD = DECIMAL 4
	0	1	0	1	BCD = DECIMAL 5 (Column 1 + 4)
	0	1	1	0	BCD = DECIMAL 6 (Column 2 + 4)
	0	1	1	1	BCD = DECIMAL 7 (Column 1 + 2 + 4)
	1	0	0	0	BCD = DECIMAL 8
	1	0	0	1	BCD = DECIMAL 9 (Column 1 + 8)

CONVERSION BCD TO DECIMAL.

To convert BCD to decimal

011001110001

divide the number into groups of 4 from right to left

0110 0111 0001

convert each binary group to a number between 0 - 9.

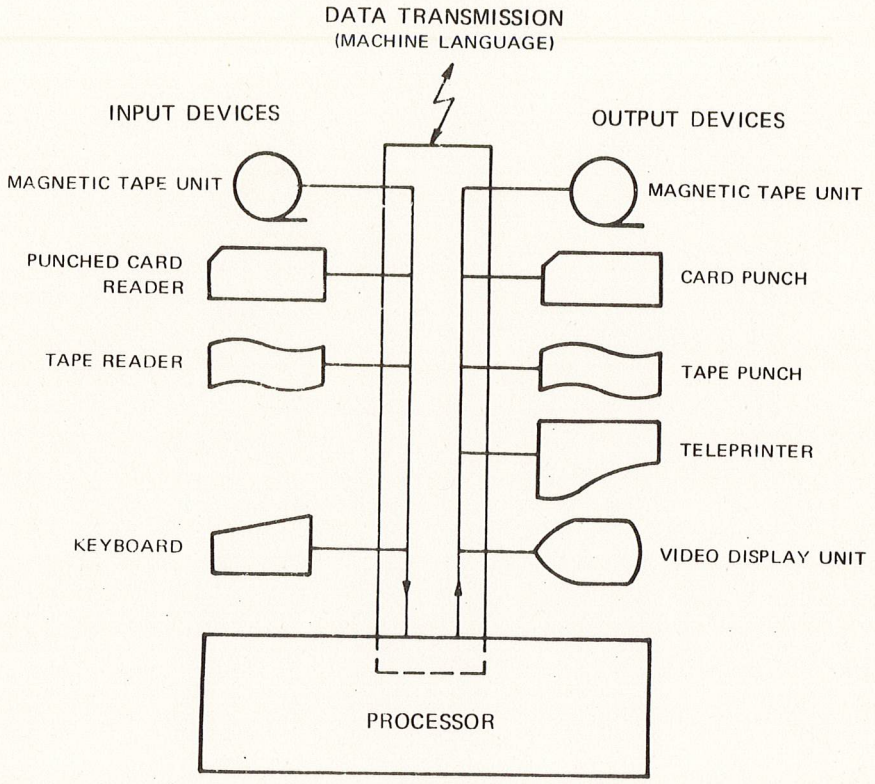
6 7 1

Decimal Number = 671

Operator Processor Communication

Communication between the processor and the operator is performed in 2 stages:-

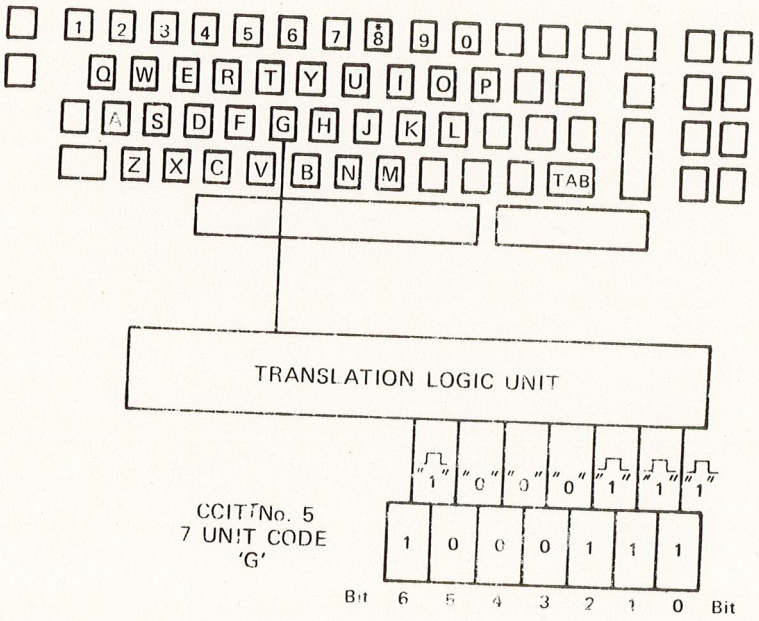
1. Between the operator and the input/output device
2. Between the input/output device and processor



EXAMPLES OF I/O DEVICES

The purpose of the input device is to translate the language used by an operator into a language that is understood by the processor (machine language). The output device, translates machine language to a form understood by the operator. Store input/output devices are made up of 95 are units, i.e. the teleprinter.

The diagram below shows an example of a teleprinter keyboard and the conversion of a letter to machine code.



TRANSLATION OF A LETTER TO MACHINE CODE

The example shown above shows the teleprinter converting to CC1TT No. 5 7 Unit Code

This code is the code to be used with ARE 11 Systems, other codes used in various systems are the ASC II Code and BCD Code.

The ASC II Code (pronounced ASKEY) is the code developed in the U.S. and is the abbreviation for the American Standard Code for Information Interchange. Figure as shown is a reproduction of a table showing the full ASC II Code.

TABLE 1: ASCII CHARACTER CODE

B6	B5	B4	B3	B2	B1	B0	COLUMN / ROW	0	1	2	3	4	5	6	7
			0	0	0	0	0	NUL	DLE	SPACE	0	@	P	\	p
			0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
			0	0	1	0	2	STX	DC2	"	2	B	R	b	r
			0	0	1	1	3	ETX	DC3	#(£)	3	C	S	c	s
			0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
			0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
			0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
			0	1	1	1	7	BELL	ETB	'	7	G	W	g	w
			1	0	0	0	8	BACK SPACE	CAN	(	8	H	X	h	x
			1	0	0	1	9	HOR TAB	EM	)	9	I	Y	i	y
			1	0	1	0	10	LINE FEED	SUB	*	:	J	Z	j	z
			1	0	1	1	11	VERT TAB	ESCAPE	+	;	K	[	k	{
			1	1	0	0	12	FORM FEED	FS	,	<	L	\	l	|
			1	1	0	1	13	CARRIAGE RETURN	GS	-	=	M	]	m	} (Alt Mode)
			1	1	1	0	14	SHIFT OUT	RS	.	>	N	^ (↑)	n	~
			1	1	1	1	15	SHIFT IN	US	/	?	O	-	o	Del (Rub Out)

ASC II CODE TABLE

This code gives a total of 128 possible ~~originals~~ characters of this total 26 are used for upper case, alphabetical character. 26 for lower case, 10 numerals (0-9), 32 special characters (commas, full stops etc.)

34 non printing control characters. The table also shows that this code is also a 7 unit code.

its b_7	b_6	b_5	b_4	b_3	b_2	b_1	Row \ Column	0	1	2	3	4	5	6	7
								0	0	0	0	1	1	1	1
								0	0	1	1	0	0	1	1
								0	1	0	1	0	1	0	1
			0	0	0	0	0	NUL	(TC,) DLE	SP	0	(@)	P		P
			0	0	0	1	1	(TC1) SOH	DC_1	!	1	A	Q	a	q
			0	0	1	0	2	(TC_2) STX	DC_2	"	2	B	R	b	r
			0	0	1	1	3	(TC_3) ETX	DC_3	£	3	C	S	c	s
			0	1	0	0	4	(TC_4) EOT	DC_4	$	4	D	T	d	t
			0	1	0	1	5	(TC_5) ENQ	(TC_3) NAK	%	5	E	U	e	u
			0	1	1	0	6	(TC_6) ACK	(TC) SYN	&	6	F	V	f	v
			0	1	1	1	7	BEL	(TC_{10})ETB	′	7	G	W	g	w
			1	0	0	0	8	FE_0 (BS)	CAN	(	8	H	X	h	x
			1	0	0	1	9	FE_1 (HT)	EM	)	9	I	Y	i	y
			1	0	1	0	10	FE_2 (LF)	SUB	=	:	J	Z	j	z
			1	0	1	1	11	FE_3 (VT)	ESC	+	;	K	([)	k	
			1	1	0	0	12	FE_4 (FF)	IS_4 (FS)	,	<	L		l	
			1	1	0	1	13	FE_5 (CR)	IS_3 (GS)	-	=	M	(])	m	
			1	1	1	0	14	SO	IS_2 (RS)	.	>	N		n	
			1	1	1	1	15	SI	IS_1 (US)	/	?	O	-	o	DEL

CC1TT NO. 5 CODE TABLE

Baudot Code

This code also called Murray Code or International Code No. 2, originated about 1906, when teleprinter machines were developed for sending out automatically encoded messages over telegraph lines. It is still in wide use throughout the world for transmission of news, services, ship/shore messages etc.

A point to note is that although a total of 57 characters may be transmitted, only 5 encoding bits are used, as the total number of combinations from 5 bits is only 32, two special control characters are used.

TABLE 2: BAUDOT CODE						
CHARACTER		CODE				
LETTERS	FIGURES	B1	B2	B3	B4	B5
A	-	1	1	0	0	0
B	?	1	0	0	1	1
C	:	0	1	1	1	0
D	$	1	0	0	1	0
E	3	1	0	0	0	0
F	!	1	0	1	1	0
G	& (OR (@)	0	1	0	1	1
H	STOP (OR£)	0	0	1	0	1
I	8	0	1	1	0	0
J	OR BELL	1	1	0	1	0
K	(	1	1	1	1	0
L	)	0	1	0	0	1
M	.	0	0	1	1	1
N	,	0	0	1	1	0
O	9	0	0	0	1	1
P	0	0	1	1	0	1
Q	1	1	1	1	0	1
R	4	0	1	0	1	0
S	BELL (OR !)	1	0	1	0	0
T	5	0	0	0	0	1
U	7	1	1	1	0	0
V	: (OR =)	0	1	1	1	1
W	2	1	1	0	0	1
X	/	1	0	1	1	1
Y	6	1	0	1	0	1
Z	" (OR +)	1	0	0	0	1
Space		0	0	1	0	0
Carriage Return		0	0	0	1	0
Line Feed		0	1	0	0	0
"Letters"		1	1	1	1	1
"Figures"		1	1	0	1	1

BAUDOT CODE CHART

4.1 SCHMITT TRIGGER (OR VOLTAGE COMPARATOR)

If a logic signal is fed down a transmission line or over a cable, it suffers amongst other things from noise, picked up along the line. A Schmitt Trigger reshapes the logic signal at the cable output so that the signal at the output of the Schmitt Trigger is the same as the signal at the input of the cable.

4.2 THE NON INVERTING SCHMITT TRIGGER

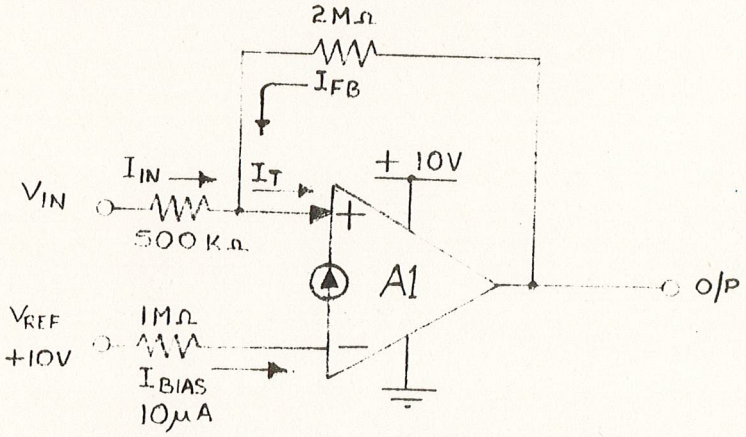
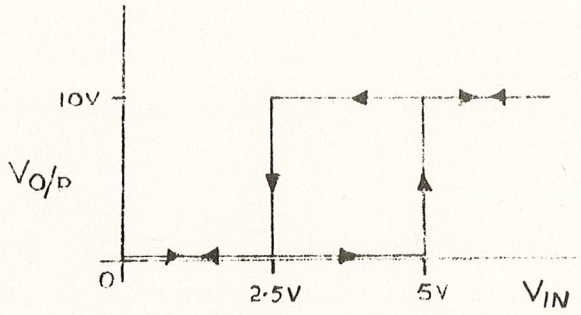


FIG. 1 THE N.I. SCHMITT TRIGGER

Amplifier A1 is a very high gain amplifier fed from a 10 volt power supply. With V_{IN} at 0V I_{IN} is 0A but V_{REF} is +10V which causes a 10μA Biss Current (I_{BIAS}) to flow into the (-) terminal of A1 this keeps the O/P at 0V and I_{FB} is therefore 0V.

As V_{IN} starts to go positive, I_{IN} starts to flow into the (+) terminal of A1. When V_{IN} gets to +5V I_{IN} is 10μA which is equal to I_{BIAS} and the O/P of A1 starts to go positive. The O/P going positive causes I_{FB} to flow which adds with I_{IN} to form I_T. The total of these two currents causes the O/P to saturate in the positive direction (+10V) and I_{FB} is now 5μA (i.e. $\frac{V\ O/P}{2M\Omega}$ = 5μA) an if V_{IN} is still 5V then I_T is 15μA (i.e. (I_{IN} = 10μA) + (I_{FB} = 5μA) = (I_T = 15μA)
As V_{IN} is reduced nothing happens to the O/P until V_{IN} reaches +2.5V. At +2.5V I_{IN} is 5μA and I_T is 10μA ($I_T = I_{IN} + I_{FB}$) and is equal to I_{BIAS} (10μA), therefore the O/P starts to go towards 0V, which causes I_{FB} to reduce which causes a further reduction in I_T until the O/P is 0V and I_{FB} is 0A making I_T equal to I_{IN} = 5μA.



Graph of V_{IN} Vs $V_{O/P}$ for the Non Inverting Schmitt Trigger.

FIG. 2

Note that Figure 2 slightly resembles the Hysteresis loop for a piece of magnetic material. This curve is also called a Hysteresis curve.

4.3 THE INVERTING SCHMITT TRIGGER

The circuit for the inverting Schmitt Trigger is essentially the same as the circuit for the non inverting Schmitt Trigger except that the V_{IN} Terminal is tied to our reference voltage V_{REF} and the input is applied to what was our V_{REF} terminal as shown in Figure 3. Figure 4 shows the curve for the Inverting Schmitt Trigger. Note the different values of components in Figure 3 compared to Figure 1.

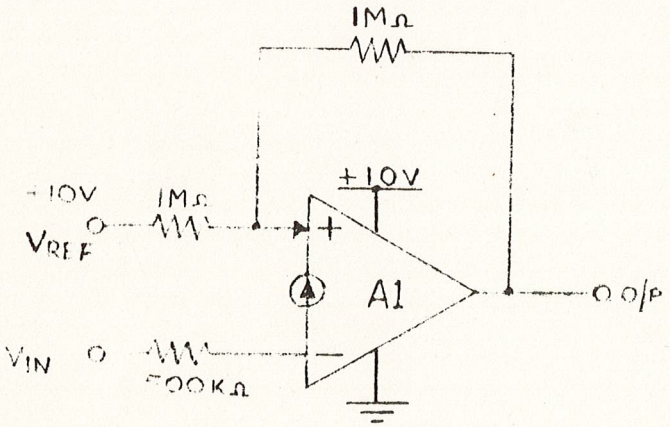


FIG. 3

CIRCUIT

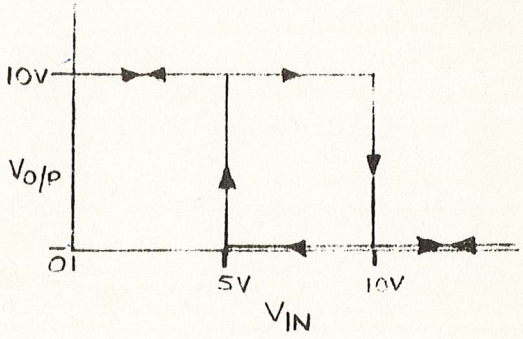
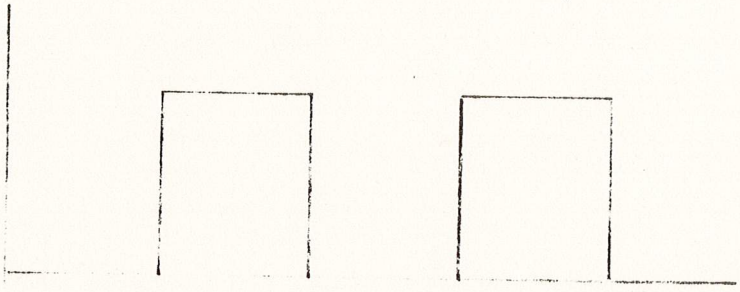


FIG. 4

HYSTERESIS CURVE

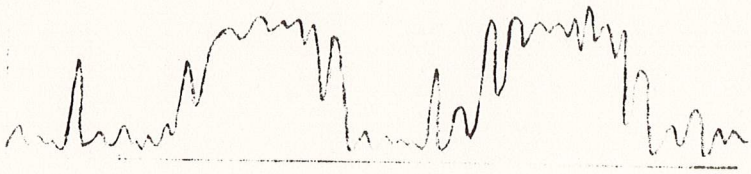
4.4 APPLICATIONS OF SCHMITT TRIGGERS

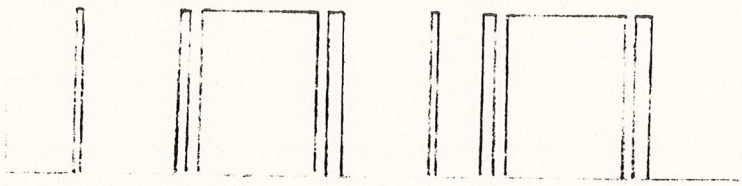
As mentioned in 4.1 a signal fed down a cable can pick up a lot of noise. If this signal is applied directly to the logic, it can cause false switching. A Schmitt Trigger can overcome this as the following graphs show.



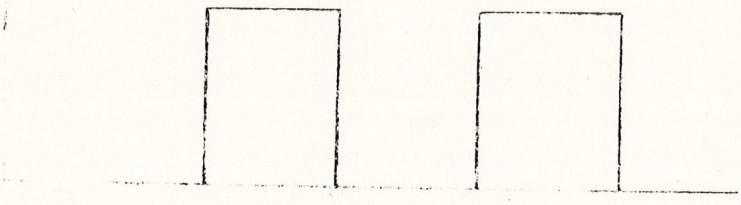
Signal applied to cable I/P.

Signal at cable O/P. Note distortion caused by noise.





O/P of logic if above signal applied directly to logic circuit.



O/P Schmitt Trigger if signal in Graph 2 applied to Schmitt Trigger Input. Note - No false switching.

COMPONENT FAMILIES

5.1 EARLY LOGIC FAMILIES

In the early days of logic, devices that performed the switching functions were often mechanical, electro-mechanical or even "fluid gates" using liquids or gases instead of electric current flow. Examples of each type of logic are:- Mechanical logic in the Babbage Analytical Engine of the early nineteenth century. Relay logic was used in a four function calculator developed at Harvard University in 1944 and fluid logic was used in the early NASA space programme computer.

MODERN LOGIC

5.2 VALVE LOGIC is only mentioned because of its historical interest as a modern logic family. It had limited use before the days of transistors, and it is interesting to note that in 1949 one of the world's first computers was built at Cambridge University, using more than 3000 thermionic valves. It had a failure rate of about 1 valve every twenty minutes.

5.3 RESISTOR TRANSISTOR LOGIC (R.T.L.)

Not the first Solid State logic, but the first commercially available in I.C. form in 1966.

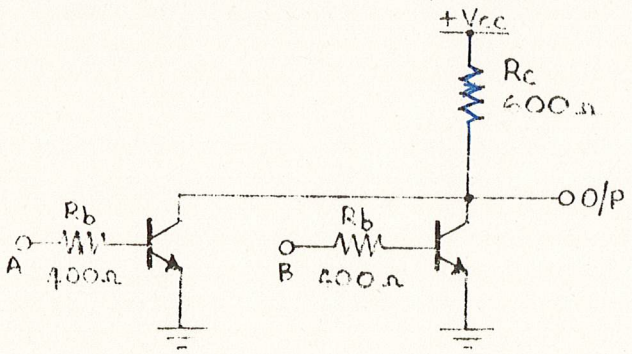


FIG. 5

Figure 5 shows the circuit to a RTL NOR gate. When either I/P A or B are at logic 1 one or both transistors will saturate and the O/P will be at logic 0. If both I/P's are at logic 0, both transistors will be cut off, and the O/P will be at logic 1, as extended from $+V_{CC}$ through the 600Ω R_C.

Due to the R.C. time constants (formed by the base resistors R6 and Base Emitter junctions) being quite large, switching time was quite slow, at up to 250nS.
The "fan out" (i.e. the number of inputs that each O/P can feed) was relatively low at 5.
This family of logic is now obsolete but may still be found in some early equipment.

5.4 DIODE TRANSISTOR LOGIC (D.T.L.)

This was the first really successful logic family to be put into I.C. form, following hot on the heels of R.T.L. D.T.L. is still produced in I.C. form today by the majority of manufacturers.

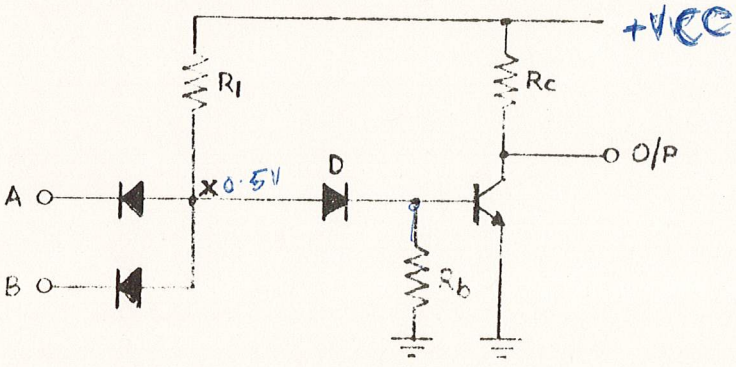


FIG. 6

Figure 6 is the circuit to D.T.L. Nand gate. With either A or B at logic 0 (ground potential), current flows from VCC, through R1, through one or both diodes to ground. Point x is at 0.6V (i.e. 1 diode drop) above ground potential. As this voltage is normally enough to turn a transistor on, Diode D is put in to ensure that the transistor remains off. With this diode (D) 1.2V is required at point x to turn the transistor on. As the transistor is off the O/P is at logic 1 as extended through RC.

If both diodes are at logic 1 (i.e. +VCC on A & B), current flows from +VCC, through R1, through Diode D and the Base-Emitter junction of the transistor, turning the transistor on. The O/P is therefore at logic 0 as extended through the transistor.

Rb is there to help the stability of the circuit and to reduce the Rb time constants, thereby decreasing switching time.

The switching time of this family is typically about 25nS and its fan out is increased to 8. It has a power consumption of approximately 10mW per gate running from a +5V supply.

5.5 TRANSISTOR TRANSISTOR LOGIC (T.T.L. or T^2L)

This is probably the most widely used logic family of them all, due to its low cost, good switching speed and moderate power consumption. This family relies on the fabrication of the multi-emitter input transistor, which can be made with very little inter-element capacitance, which act as diodes. (see figure 7) The input to this family is thus identical in operation to the D.T.L. input circuit as shown in Figure 7.

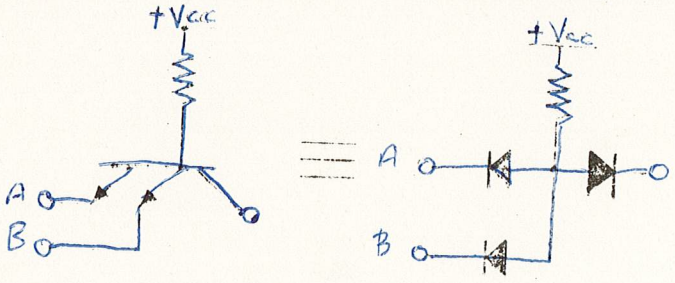


FIG. 7

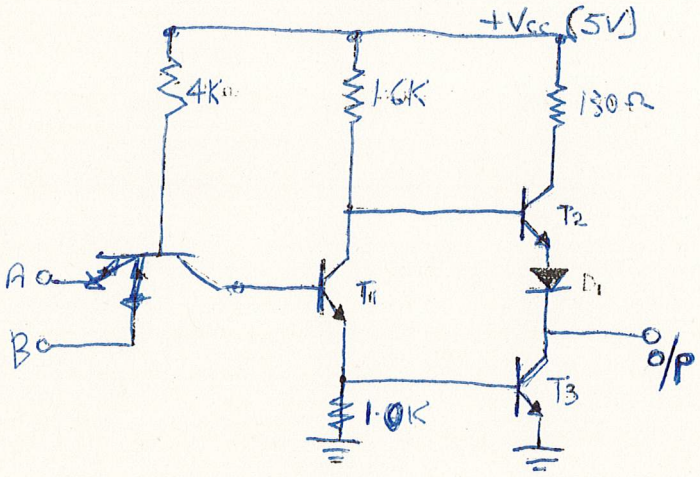


FIG. 8

Figure 8 shows the full circuit to a T.T.L. two input NAND gate.
If any I/P is at logic 0 the Base of T1 will be at logic 0 and T1 will be cut off. This will cause T3 to be cut off and T2 will be turned ON. Logic 1 will now appear at the O/P terminal via D1, T2 and the 130Ω resistor. If both I/P's are at logic 1, the base of T1 will be at logic 1 and T1 will turn on. This will cause T3 to turn on, but as T2 needs 1.2V between the O/P terminal and its base to turn on and the voltage at T1 collector is less than this (due to 0.6V B-E drop of T3 and T1 E-C saturated) T2 is turned off. The O/P is therefore at logic 0 as extended through T3.

As the input transistor can be manufactured with less inter-element capacitance than individual diodes the switching time is decreased. Note also the output configuration. This is known as a "Totem Pole, Pheonix Output". Its advantages are that there is always a low impedance path to either logic 1 or logic 0, therefore increasing fan-out, and also that it tends to "pull" the output to its appropriate logic level, again decreasing switching time.

This family can switch in about 13nS, has a fan out of 10 TTL gates and typically uses 11mW.

Its disadvantages are that it is very easily destroyed by soldering into circuits or if the voltage exceeds 5.5V at any I/P or at the supply. Several other versions of this family exist and they all use the same circuit as in Figure 9, but with some values changed for reasons as set out below.

TTL "H" Series - with all the resistor values reduced to increase speed by decreasing the time constants. The "H" stands for "High" speed, and it can switch in 7nS but consumes 40mW per gate.

TTL "L" Series - This is the "low" power version of TTL and is achieved by increasing the resistor valves. This also increased switching time to 25nS but power consumption is down to 1mW per gate.

TTL "S" Series - Schottky technology is employed in this series of gates, to increase speed to 3nS. Power consumption is 19mW.

TTL "SL" Series - Is the latest of the TTL series gates, and as the name implies, incorporates the "Low" power advantage of "L" series with the speed of "S" series to obtain a switching time of 13nS for 1mW per gate of power.

All the above derivations of the basic TTL use the same supply voltage (i.e. +5V) as standard TTL and have the same fan out (i.e. 10) into the same series, but fan out varies if fed into a different series.

e.g. TTL "L" has a fan out of 10 into TTL "L" but a fan out of 2 into standard TTL.

5.6 EMITTER-COUPLED LOGIC (ECL)

Most logic families operate in a saturated state. In order to go from one logic state to the other we must therefore wait for the full rise or fall time, (e.g. 0 to 5V) as in Figure 9. As E.C.L. operates over only part of the linear region of the transistors, the switching time is greatly reduced as shown in Figure 10.

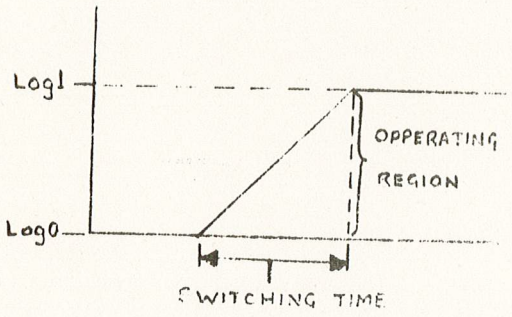


FIG. 9

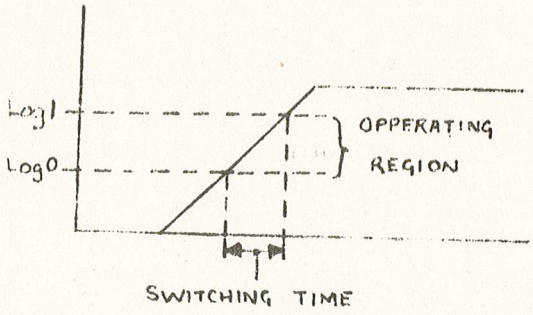


FIG. 10

The voltage difference between logic 1 and logic 0 is typically only 0.8V and this makes it the fastest logic family available at present. Switching time is typically 2nS and can be as low as 1nS with some gates.

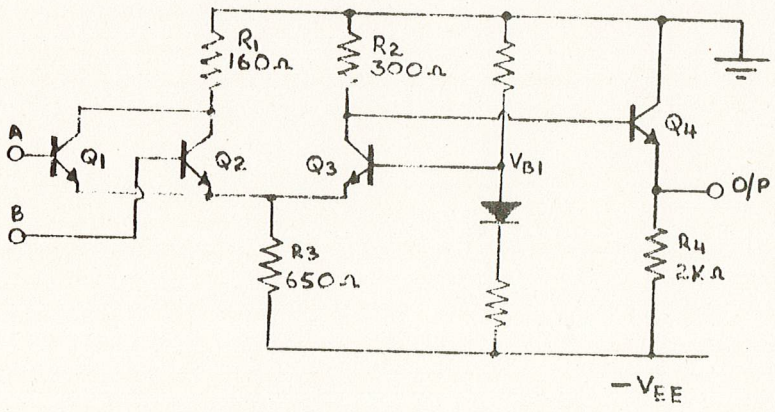


FIG. 11

Figure11 shows the circuit to an ECL gate. Point VB1 is held at -1.04 Volts. When either A or B go to logic 1 which is -0.81 volts either Q1 or Q2 conducts harder (see figure 10). This will raise the potential at the top of R3 and Q3 will switch off slightly. This will cause the potential at Q3 collector to increase, therefore Q4 will switch on slightly (see figure 10) and a logic 1 (i.e. -0.81V) will appear at the O /P.

If both A & B go to logic 0 which is -1.65V Q1 and Q2 will turn off slightly, therefore the potential at the top of R3 will decrease. This will cause Q3 to turn on harder and the potential at the collector of Q3 will decrease slightly as per Figure 10. This will cause Q4 to turn off slightly and the O/P will go to logic 0, which is -1.65V.

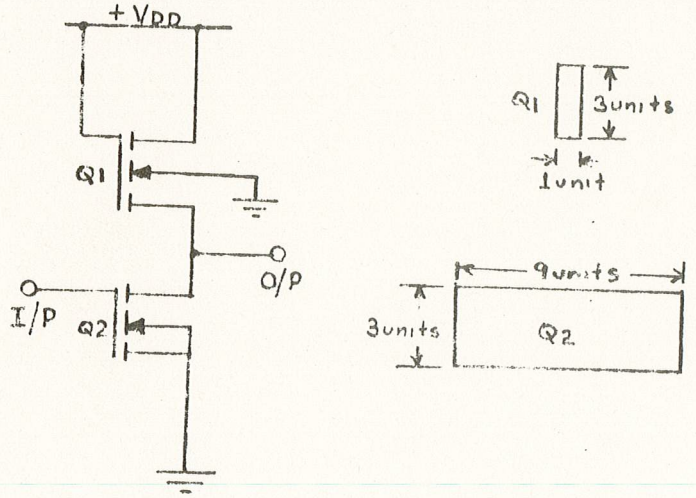
Note that this family is still positive logic as logic 1 (-0.81V) is more positive than logic 0 (-1.65V).

The limited logic swing (0.8V) which allows this family to achieve its speed, also makes it very noise prone and special shielding should be used with E.C.L.

Apart from its speed, the other advantage of this logic family is its high fan out of 30, made possible by its emitter follower output stage. Power consumption however, is very high at around 65mW per gate. This only makes E.C.L. suitable for Small Scale Integration (SSI) defined as less than 13 gates per I.C. Any more gates than this would cause overheating of the I.C.

5.7 METAL OXIDE SEMI-CONDUCTOR (MOS)

This technology is mainly used in Large Scale Integration (L.S.I. defined as over 100 gates per chip) and this made possible the hand held pocket calculator, the micro-processor and large solid state memories, where thousands of gates are formed on one chip. The reason that such high density is possible is that only one type of element is manufactured, varying only in physical size.



(A) CCT. (B) ELEMENT SIZE

FIG. 12 MOS INVERTER

Figure 12 shows the MOS inverter. Q1 is held on constantly, and acts as a resistor. Q2 is switched on and off at will and is the element that does the switching.

When the I/P is taken to logic 1 (+vDD), Q2 switches on. Because of its relative width with relation to Q1 (see Fig. 12B) its resistance is approximately $\frac{1}{9}$ that of Q1, and the O/P will appear close to earth potential. If the I/P is taken to logic 0 (earth) Q2 will switch off, and logic 1 will be extended to the O/P via Q1. Figure 13 shows the MOS Nor gate. These gates are not produced in S.S.I. I/C's but only as a part of a much longer circuit as mentioned earlier.

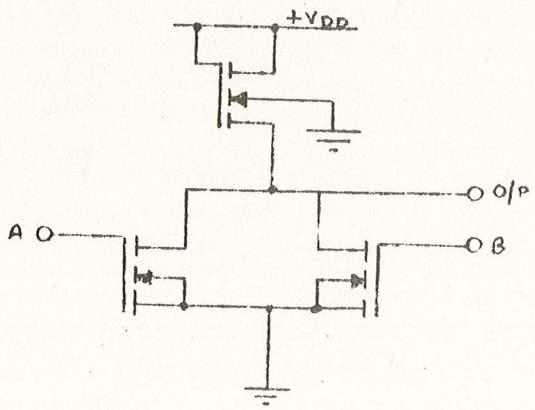


FIG. 13 MOS NOR GATE

The advantage of MOS is its simplicity of production and its very high fan out within the family. Fan out however drops to only a few gates when fed into T.T.L. or D.T.L.

Its main disadvantages are that MOS is very static prone (as are most FET devices) and can be destroyed simply by touching its leads. For this purpose MOS I.C.'s are, prior to leaving the factory, packed in conductive foam which shorts all leads together. Special precautions must be observed when soldering, that we solder the earth lead first then the battery lead, then all the other leads, with the tip of the iron earthed to the I.C. earth. Also don't wear nylon clothing near MOS devices as static from a charged shirt can induce a charge on the I.C. leads and destroy the device. Its other disadvantage is that some MOS devices require a dual power supply, typically, -12V and +15V.

5.8 COMPLEMENTARY METAL OXIDE SEMI-CONDUCTOR (C.M.O.S.)

This family of logic is pin for pin equivalent to TTL but not compatible to it. It has been described as the most elegant of logic families due to its low power consumption, in the order of 10nW per gate and high fan out, as high as 1000. In all regards it is the almost perfect static switch, which can operate at any voltage between 3V and 15V. From the circuit given in Figure 14 of a CMOS inverter it is noticed that one element (Q2) is an N channel FET while the other (Q1) is a P channel FET. Hence the name COMPLEMENTARY. With the I/P taken to logic 1 (+VCC) the top element (P channel) is switched off while the bottom element (N channel) is switched on. Logic 0 is therefore extended to the O/P. If the I/P is taken to logic 0 (ground) then the bottom element (N channel) switches off and the top element (P channel) switches on, extending logic 1 to the O/P. Notice that at no time does current flow in this circuit, with the exception of leakage current, which is in the order of 1nA, and a slight current at the instant of switching. This is when one element is turning off, while the other element is turning on. The power consumption of CMOS therefore increases as the rate of switching increases, but is only in the order of micro-watts when switched at MHz rates.

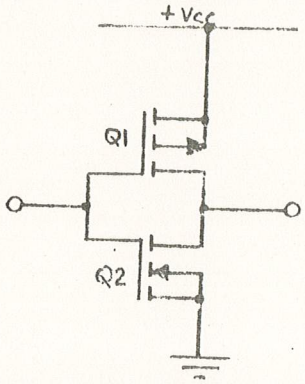


FIG. 14 CMOS INV

As the input impedance is in the order of 10^{12}ohms any capacitance at the gate produces long time constants and the switching time of CMOS is approximately 50nS.

This is still much faster than the MOS family of gates for the same reason that Totem Pole TTL was faster than DTL (Ref. Section 5.5). It does however suffer the same major disadvantages of MOS, that it is very prone to static charges and therefore the same static precautions must be observed with CMOS as with MOS. On the advantage side is its

low power consumption and its high noise immunity of 0.45 VCC. This means that if +VCC is +10V, its I/P must go to +4.5 before the output starts to switch and completes its switching when the I/P voltage is +5.5V. Apart from this timers can very easily be constructed (see Figure 16) and LED's can be driven directly without need for any other components.

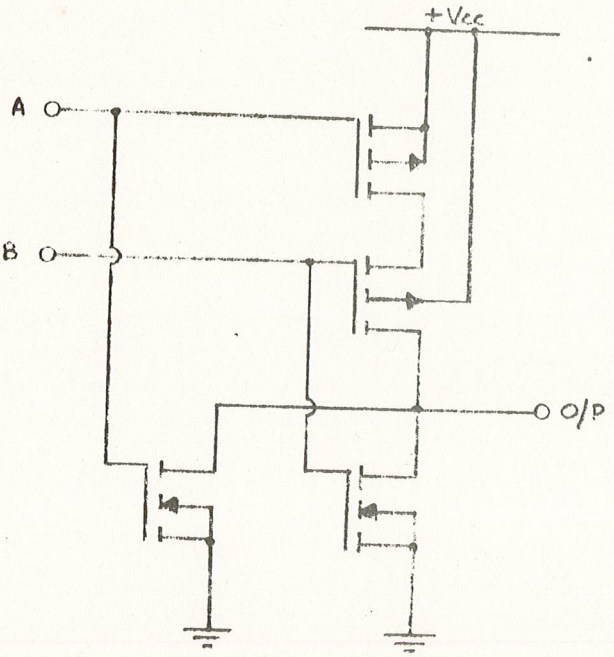


Figure 15 shows the circuit to a CMOS NOR gate. Note once again that current never flows in this circuit except at the instant of switching.

FIG. 15 NOR GATE

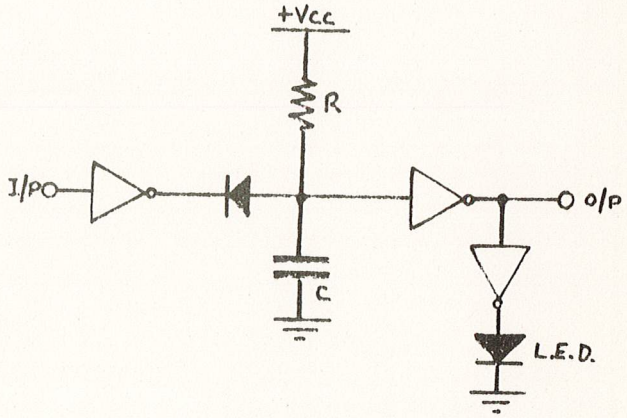


FIG. 16 SIMPLE TIMER

5.9 INTEGRATED INJECTION LOGIC (I^2L)

At the time of writing (mid 1977) not much information was available on I^2L as it is a fairly recent family. We do know however that it lends itself to L.S.I. and that a whole digital watch including readout can be built on a single chip. This type of logic is also known as Merged Transistor Logic (M.T.L.).

I^2L is the IBM name given to it and NTL is the Phillips name given to it. Both these companies came up with the same circuit at the same time but working quite independently from one another(?) Figure 16 shows the circuit to a I^2L NOR gate. Note the multi collector transistors for multiple outputs. Yes all transistors act as transistors in this family. Transistors Q1, Q2 & Q5 act as constant current sources and are called "Current Injectors" from which the family gets its name. With A & B left open circuit the current flows from VCC, through Q1 & Q2 to Q3 & Q4 causing Q3 & Q4 to switch on.

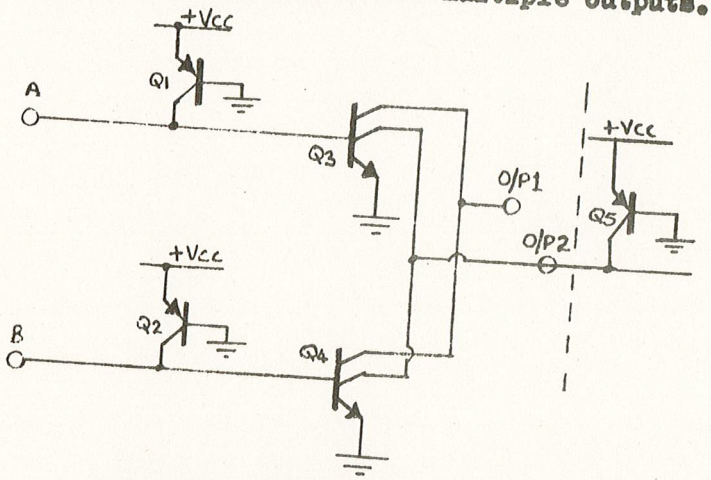


FIG. 16 I^2L GATE

This will shunt the current that flows through Q5 to earth and a logic 0 is placed on the O/P2. Note that Q5 is actually in the next gate. With A & B at ground potential the currents that flow through Q1 & Q2 are shunted to ground and therefore Q3 & Q4 are switched off. The current that flows in Q5 now is allowed to flow into the base of the next transistor (not shown), representing a logic 1 at O/P2.

Logic 0 is therefore an earth on the I/P while logic 1 is an open circuit input.

The advantages of this circuit are that as we have moved the load resistance out of the gate output circuit, and into the next gates input circuit, therefore the power consumed in a gate is proportional to the number of other gates it feeds. Also the Current Injectors can be made variable so that for low speed operation only a low injection current is used and for high speed operation, a higher injection current is used. Unlike CMOS however, where the speed determined the current drain, in I^2L the current drain determines the speed. For low speed operation, these gates can work with nW of power.

Their main disadvantage is that the O/P voltage swing is only about 0.6V, making this logic very noise prone.

5.10 CONCLUSION

The families described above are not all that exist. Some are so obsolete that they were not discussed and some so new that nothing is yet known about them. However, the ones discussed are the more likely ones we will encounter at present and for quite a few years to come. This is both on the job as Telecom employees and in our everyday lives, as logic plays a greater part in home appliances. Also many of us may use logic in one of its many forms in our hobbies. It is hoped that this section may help you in whatever application you encounter logic circuits.

LOGIC COMPONENTS 2

6.1 INTRODUCTION

It is often necessary to come out of a logic cct. and drive some form of display, cable or other logic family whose I/P is not compatible with the previous families' O/P. Sometimes many gates can be saved by using simple techniques available to us in some of the families. At other times we may require information about a particular type of I.C.'s behaviour.

This section will discuss the above points and demonstrate how to achieve them.

6.2 INTERFACE CCTS.

These are used when we come out of a logic cct. and want to feed a cable, lamp or electro-mechanical device. They are also used if a gate has to feed such a large number of other gates, that its fan out is exceeded or when going from one logic family to another, working at the same or different supply voltages.

In Figure 17A we have the cct. to an interface cct. for getting from TTL or DTL into P channel MOS. Figure 17B shows the connections for this cct., which is called a "Dual Voltage Translator".

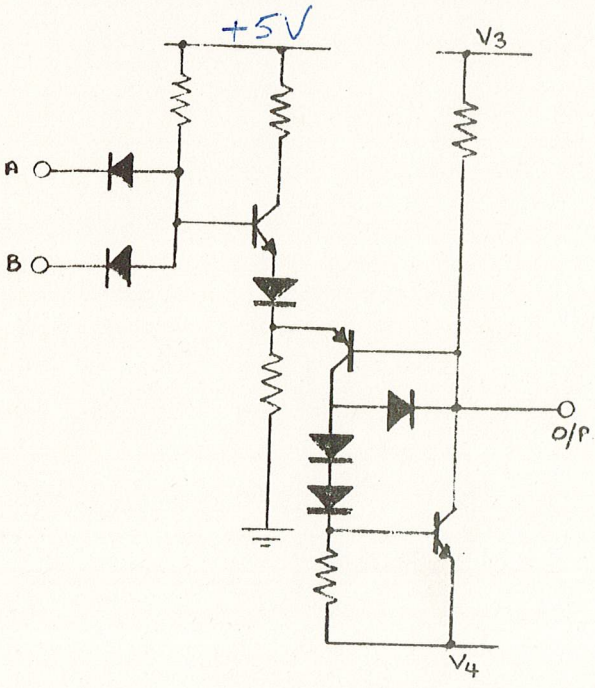


FIG. 17A

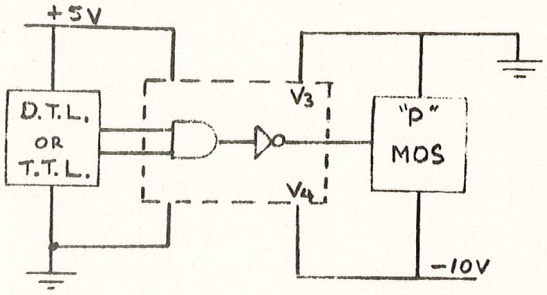


FIG. 17B

This circuit can also be used to interface between TTL/DTL and other families (e.g. CMOS) simply be re-arranging V3 and V4 for the appropriate earth level, and correct supply voltage.

Other interface circuits exist for interfacing between logic circuits of the same or different families, apart from the one shown here. It is often necessary to interface between logic and other devices. Figure 18 shows a circuit that allows us to do this. G1 is a standard TTL gate coupled to a power transistor Q1 in the same I.C. package. Two of these circuits are available in the one I.C. Once again two supply voltages are used. One for the logic and one for the driven device. These voltages may be the same or they may differ, as long as they are both the same polarity as the earth is common. These circuits are generally called "Drivers."

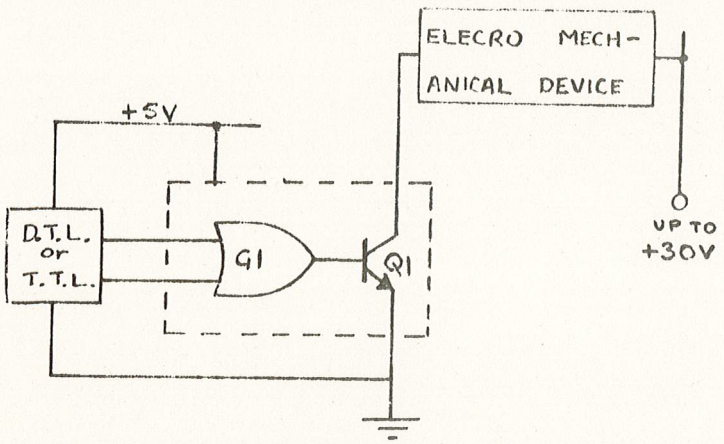


FIG. 18

Buffers are just like normal gates but the output transistors or FETS are capable of withstanding higher currents. In some circuits the O/P circuit may differ slightly from the standard circuit. These are used mainly to drive a large number of gates, and their switching speed is usually slower than that of their standard counterparts.

6.3 WIRED GATES (OR PHANTOM GATES)

It is often possible to reduce the total number of gates in a logic circuit by strapping the O/P's of several gates together. This eliminates one gate and reduces the total component count of the circuit. If this is done a number of times on a circuit the total saving can be considerable.

If we simply tried to wire the O/P's of two TTL gates together however, when one gates O/P is logic 1 and the other gates O/P is at logic 0, we risk damage to the O/P stage of the TTL gates. For this reason when we use wired gates we must use "Open Collector" gates for the TTL family. Figure 19 shows an open collector TTL gate.

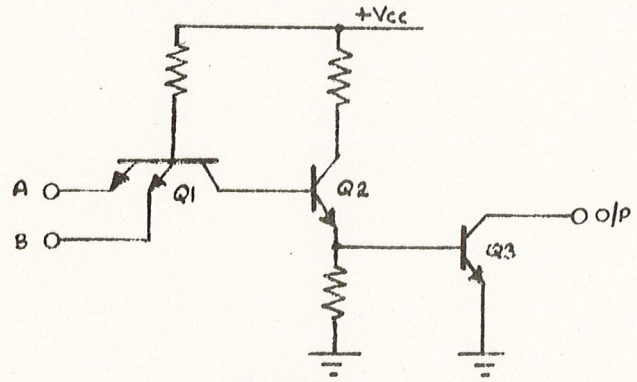


FIG. 19

Note in this circuit that the top Totem pole Transistor and diode have been removed, and that the collector of the O/P transistor Q3 has been left open circuit. Hence the name "Open Collector" gates. To use these gates, a resistor has to be wired from the O/P to the +VCC to act as a full up resistor. The circuit to a wired gate is shown in Figure 20. In this circuit we see the two output transistors belonging to two "Open Collector" gates "Wired Together". The function at the O/P is the AND function, as both transistors have to be off for a logic 1 at the O/P. In spite of this the circuit is often called a "Wired OR" and shown as in Figure 21 together with the Boolean expressions that demonstrate why it is called wired OR.

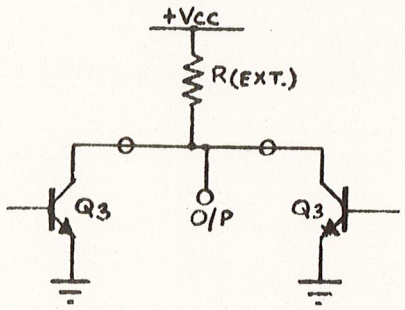
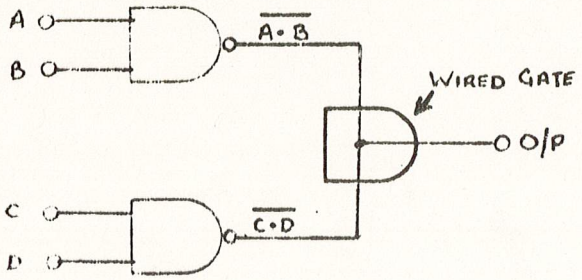


FIG. 20



$$O/P = \overline{A \cdot B} \cdot \overline{C \cdot D}$$

$$= \overline{A \cdot B + C \cdot D}$$

FIG. 21

Open collector gates are about 50% slower than normal "Totem Pole" gates and take approx. 17nS to switch. However, overall there is a time saving because if we used a standard AND gate in Figure 21 instead of the Wired gate it would take the logic a total of 22nS to propogate from the I/P's to the O/P. Using the Wired gate reduces this time by 5nS as the logic only has to propogate through 1 gate instead of 2.

In some families "Open Collector" gates are not possible. An example of this is the CMOS family (Ref. 5.8). Because of this, if a wired gate is required we must use gates with a "TRI-STATE" I/P. This Tri-State I/P when at logic 1, makes the O/P of the gate look like an Open circuit. Therefore it does not matter if we take the O/P to logic 1 or 0 via the O/P of another gate. This principle is demonstrated in Figure 22. If I/P's A & B are opposite logic levels and we make C a logic 1, the O/P of gate A will appear Open circuit. If D is at logic 0, then the O/P of B will be the inverse of B, and because A is open circuit the level at the O/P will be the same level as gate B O/P. Note the Tri-State lead shown going into the side of the gate as opposed to the normal I/P leads.

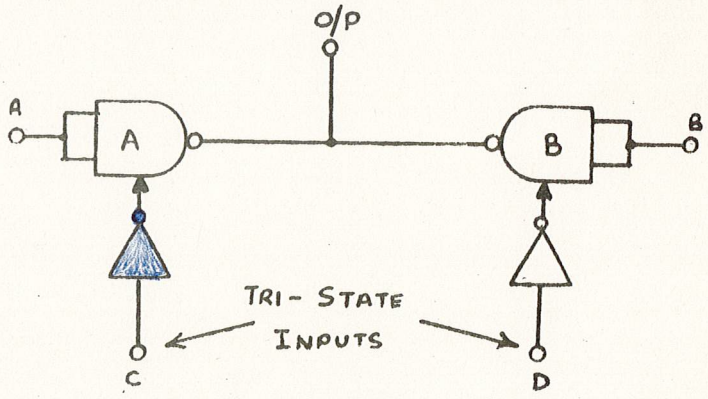


FIG. 22

6.4 EXPANDABLE GATES

Often the number of inputs the manufacture provides on a gate is insufficient for the job required of the gate. For this reason when using D.T.L. gates we have a choice of "expandable" gates. These gates have an "EXPANDOR" lead coming out to which we can attach extra diodes, in order to increase the gates number of I/P's. Figure 23 shows a D.T.L. gate with expandor input. The two external diodes C & D may either be normal diodes or they may be purchased in I/C form, and are called the "expandor gate". It will be noticed from Figure 23 that the expandor I/P has no diode. The reason is that point x should only be one diode drop above earth potential for reliable switching. The symbol to an expandable gate is shown in Figure 24. Note how the expandor I/P is shown and designated on this symbol.

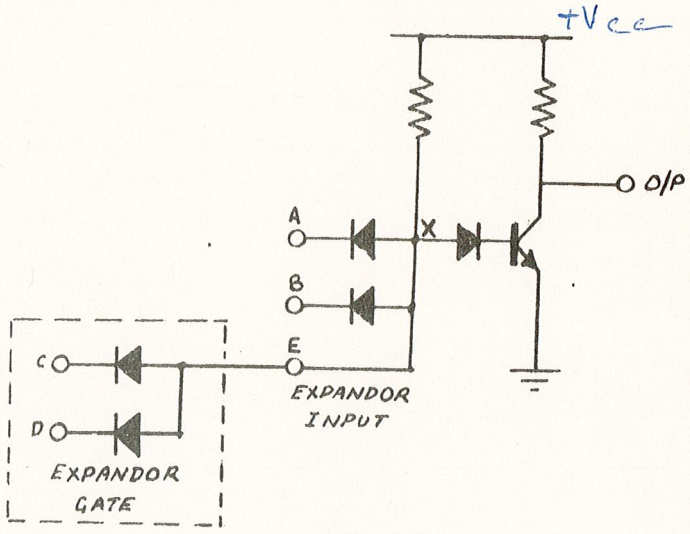


FIG. 23

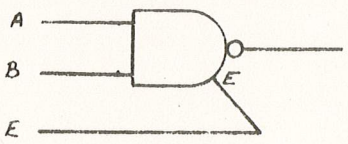


FIG. 24

Reasons for using expandable gates are that we may require more inputs in a gate or that the expandor gate may be remote from the expandable gate. It should be noted that by using these gates, overall propogation delay is reduced over using a number of gates.

6.5 MANUFACTURERS DATA

Quite often it is necessary to refer to manufactures manuals in order to find out about a particular I.C. This could be while fault finding when designing or modifying logic circuits or when a particular I.C. becomes unobtainable and a substitute or equivalent has to be found. The Manufacturer data gives us this information and in this section an outline is given on what the data tells us.

6.5 (i) DEVICE NUMBER

In this number is contained the device family and the logic functions. Either side of this number there may be several letters or other numbers. These are codes which vary between the manufacturers, and are detailed in the various manuals.

54/74 Series These devices start at 5400 and 7400. The 54 indicates that the IC is made to military specifications whereas the 74 indicates industrial specifications. The two digits after the series (e.g. 00) tells us the type of logic function performed by the I/C. Hence the only difference between a 7400 and a 5400 is its environmental specs. Often I.C.'s that do not meet 54 series specifications are marketed as 74 series.

54H/74H Series (e.g. 54H00 or 74H00) This is the high speed version of the standard 54/74 TTL series above.

54L/74L Series (e.g. 54L00 or 74L00) This is the low power version of the standard 54/74 TTL series above.

54S/74S Series (e.g. 54S00 or 74S00) This is the Schottky version of the standard 54/74 TTL series above.

54SL/74SL Series (e.g. 54SL00 or 74SL00) This is the low power Schottky version of the standard 54/74 TTL series above.

54C/74C Series (e.g. 54C00 or 74C00) This is the CMOS family version of the TTL series I.C.'s.

All the above I.C.'s are pin for pin equivalents but are not necessarily compatible between series. (i.e. a 74C00 has the same pin connections as a 7400 but might not work in place of a 7400).

930 Series is the DTL version of I.C.'s and typical device numbers are 930, 932, 957 etc.

9000 Series this is an early version of TTL. Its circuits vary slightly from 54/74 series TTL and is rarely seen.

10000 Series is the ECL series of I.C.'s.

4000 Series is the earlier version of the now popular 54C/74C CMOS Series, except that the pin connections are different. In the 4000 series 4000M indicates military specs while 4000C indicates industrial (or commercial) specs. Some MOS devices are also 4000 series devices and care should be taken when consulting manuals. However the alphabetical prefix is different between CMOS and MOS. For example a National CD4010 is a CMOS Hex Buffer while a National MM4010 is a MOS Dual 64 Bit Accumulator.

5000 Series is purely MOS devices.

VCC or VDD is the Positive or Negative supply voltage and is usually specified as a Typical, Min and Max valves, for both the Industrial and Military specifications.

6.5 (ii) OPERATING TEMP. RANGE

Is not given a symbol and is specified in the same manner as the supply voltage. Some manufactures, however, only give a Max and Min temperature and omit the Typical.

6.5 (iii) ABSOLUTE MAXIMUM RATINGS

Is only given by some manufacturers. The ratings where given include maximum voltage, operating and storage termperature and soldering temperature and time. If these ratings are exceeded the I.C. could be destroyed or at least, some how damaged.

6.5 (iv) RECOMMENDED OPERATING CHARACTERISTICS

Are given by all manufacturers and are the guaranteed levels at which the I.C. will work.

6.5 (v) FAN OUT

Is given as the number of "Unit Loads" a gate can feed. One unit load is defined as 1 normal I/P in the same logic family. Each I/P to a Nand gate would therefore present a Unit Load of one, while the Clock Input to a J.K. flip-flop would present a Unit Load of 3, as this I/P feeds three Nand gates within the flip-flop.

6.5 (vi) HIGH AND LOW LOGIC LEVELS

The manufacturer often specifies his data sheets in this fashion. A high logic level would represent a logic 1 in positive logic and logic 0 in negative logic, while a low logic level would represent a logic 0 in positive logic or a logic 1 in negative logic.

The following descriptions are written for positive logic as it is the most common type used.

VIH or Input HIGH Voltage Is given as the lowest voltage that any I/P will recognise as a logic 1. Only a minimum figure is given for this.

VIL or Input LOW Voltage Is the maximum voltage that any I/P can recognise as a logic 0. Only a maximum figure is given for this.

VOH or Output HIGH Voltage Is generally only given as the minimum voltage at the O/P for the O/P to be at logic 1. Sometimes a typical voltage is also given.

VOL or Output LOW Voltage Is the maximum voltage present at the O/P with it in the logic 0 state. A typical figure is sometimes given for this, but not always.

IIH or Input HIGH Current Is the current flowing into the input when the I/P is at logic 1. If this value has a negative sign it indicates a current flowing out of the input.

IIL or Input LOW Current Is given as a negative value and indicates current flowing out of the I/P with the input at logic 0.

ICCH or Supply Current HIGH Is either specified for each gate in an I.C. or the complete I.C. The manufacturer will indicate how this is specified. It is the current that the gate or gates draw from the supply with their O/P's at logic 1.

ICCL or Supply Current LOW Is specified in the same manner as ICCH (above) but with the O/P's at logic 0.

IOS or Output Short Circuit Current Is the current that can flow from O/P to earth with the O/P at logic 1. With some families this cannot be done and this figure is not given.

SWITCHING CHARACTERISTICS Are given under specified temperature, load resistance and load capacitance conditions.

tPLH or Turn OFF delay, Input to Output Is the time required for the output to go from logic 1 after the I/P has been switched.

tPHL or Turn ON delay, Input to Output Is the time required for the O/P to go to logic 0 after the I/P has been switched.

AVERAGE PROPOGATION DELAY Is not often given but is the average of the above two sets of figures.

NOISE CONSIDERATIONS

7.1 EFFECTS OF NOISE

In an audio system, noise is generally just a nuisance. Its degree varying with its amplitude. In a digital system, noise may either have no effect, and then above a certain amplitude its effects, QUITE SUDDENLY become disastrous, causing false switching in the system.

7.2 NOISE MARGIN

This is the "Safety Zone" incorporated into the design of logic I.C.'s and is the maximum amount of noise the circuit can SAFELY tolerate without switching. Any amount of noise in access of the noise margin may cause the circuit to switch.

FIG. 25

Figure 25 shows any two logic gates connected by a length of cable. It is within this cable that most noise is picked up. If the logic 1 O/P of gate 1 is 2.4V (see Figure 26) and the minimum allowable logic 1 input of gate 2 is 2V, then we have an 0.4V noise margin. Also if the logic 0 O/P of gate 1 is 0.4V and the maximum logic 0 Voltage of gate 2 is 0.8V, we again have an 0.4V noise margin. Any noise in access of 0.4 volts, picked up on the connecting cable could, therefore, cause the Input voltage of gate 2 to go into the indeterminate region and the gate could switch.

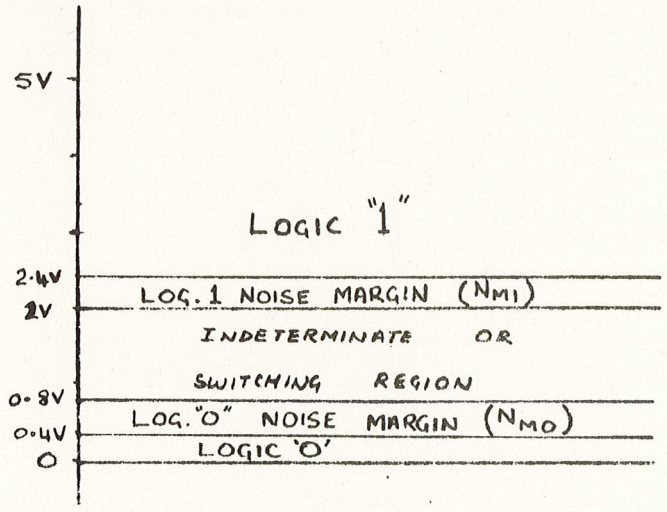
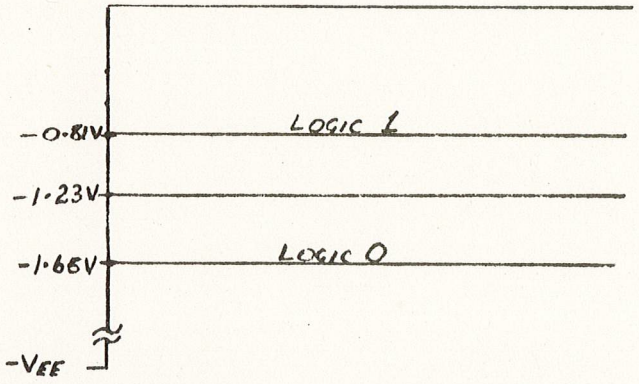


FIG. 26

The above figures are from the manufacturers data for the TTL family. Figure 26 only shows the minimum noise margin. The typical switching point of such a TTL gate is at 1.4V giving a typical noise margin of 1V.

This is not the case with all logic families. E.C.L. is very critical of noise and has a maximum noise margin of 0.4V. Note in Figure 27 that the Indeterminate zone for a E.C.L. gate does not exist. Any noise greater than 0.42V will cause this family of gates to switch. Switching occurs at -1.23V. These gates are therefore more susceptible to noise than are gates in any other family.



7.3 NOISE PROTECTION

With E.C.L. it is necessary to adequately shield all the components in the logic circuit, use shielded cable for interconnection and adequately decouple the supply lines where they enter the logic boards.

T.T.L. is not so critical, but as it generates an appreciable amount of noise on the supply line it is not uncommon to see TTL circuits with a decoupling capacitor (typically 0.01 to 0.1μf), between the VCC and earth pins of every I.C. to remove any noise from the supply line. This is not the case with MOS and CMOS, but as these families of logic are very static prone, some form of isolation is generally included between the logic and external circuit. This may take the form of a decoupling circuit, a relay or an opto isolator (L.E.D. and photo transistor).

7.4 CONCLUSION

The manufacturer does not always quote a noise margin but it can easily be found as shown above. The type of family we choose for a particular application may well depend on the noise margin of that family, if speed or power is of no concern. If E.C.L. must be used then elaborate precautions must be taken to exclude noise. If we could use CMOS then noise probably won't have any effect because of the high noise margin of this family.

Section 8

Arithmetic Circuits

As already seen it is possible to perform subtraction by taking the twos complement of the number to be subtracted and added. It is also possible to perform binary multiplication by repetitive addition and binary division by repetitive subtraction. Hence a circuit designed to perform binary addition may be used to perform virtually all of the basic arithmetic functions and this is very often done.

From a practical point of view this means that binary adder circuits tend to form the backbone of digital arithmetic hardware, so that if you have a basic understanding of adders and the way they are used you should find it fairly easy to find your way through most arithmetic problems.

Half adders and full adders are dealt with in ETP 2072 12.6 and 12.7. This section should be revised before going further.

The half adder is so called because it is only capable of adding the least significant bits of two numbers whereas to add the next most significant bits you would have to contend with a possible carry from the L.S.B. adder. Therefore for full adder operation three inputs have to be taken into account the addend, the augend and the carry from a previous stage.

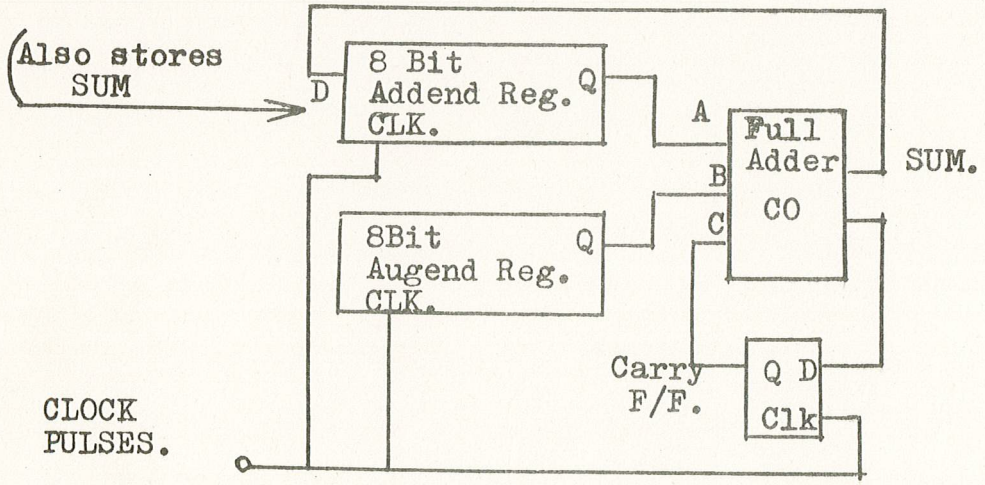
There are two ways in which two multi bit numbers may be added together.

(a) Serial or bit by bit approach

(b) Parallel or all bits at once approach

The serial approach is relatively low in cost but rather slow, the parallel approach is fast but tends to be much more costly.

Typically, serial binary addition involves a single full binary adder through which the addend and augend numbers are passed bit by bit and corresponding bits together starting with L.S.B.'s.



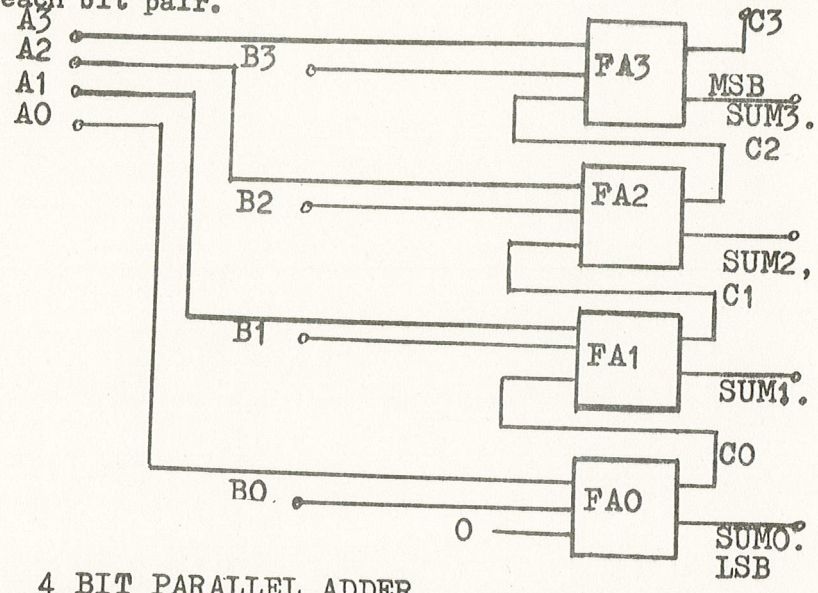
8 BIT SERIAL ADDER.

Usually the two numbers are shifted into the adder from a pair of shift register with the sum output of the adder is fed to either a third shift register or back into one of the original registers (usually the addend). A single flip flop is used to store the carry over.

Parellel Addition

Considerably faster addition is obtained by using the parallel approach because all bit pairs are added simultaneously. This also makes the addition largely independent of number size.

Basically, parallel addition involves a set of full adders working in parallel one for each bit pair.



4 BIT PARALLEL ADDER.

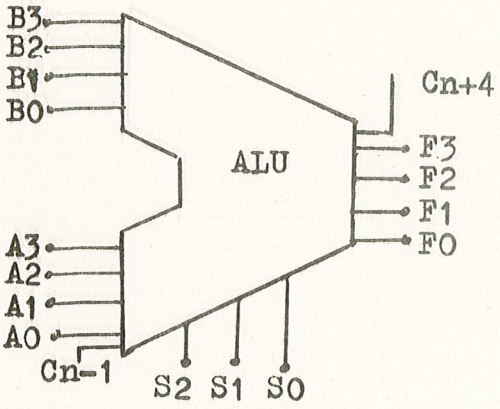
Shown above is a four bit parallel adder, using four full adder circuits the lowest adder takes the L.S.B.'s of the two input numbers. A0 and B0 and produces the appropriate sum and carry out (C0). The C.O. from FA0 is used as carry in of FA1.

If a four bit parallel adder like that shown above is used in a system dealing solely with four bit numbers the carry input of LSB adder would be disabled with a logic 0 level. Similarly the carry out-put of a FA3 would probably be left unused. However the existence of this input and output does allow a number of such circuits to be used together to handle larger numbers.

As you might expect the two adders dealt with above can be used to perform subtraction by twos complement by forming the number to be subtracted into its twos complement before adding normally.

A.L.U. Arithmetic and Logic Unit

This is a unit containing adders plus additional circuitry to perform various functions.

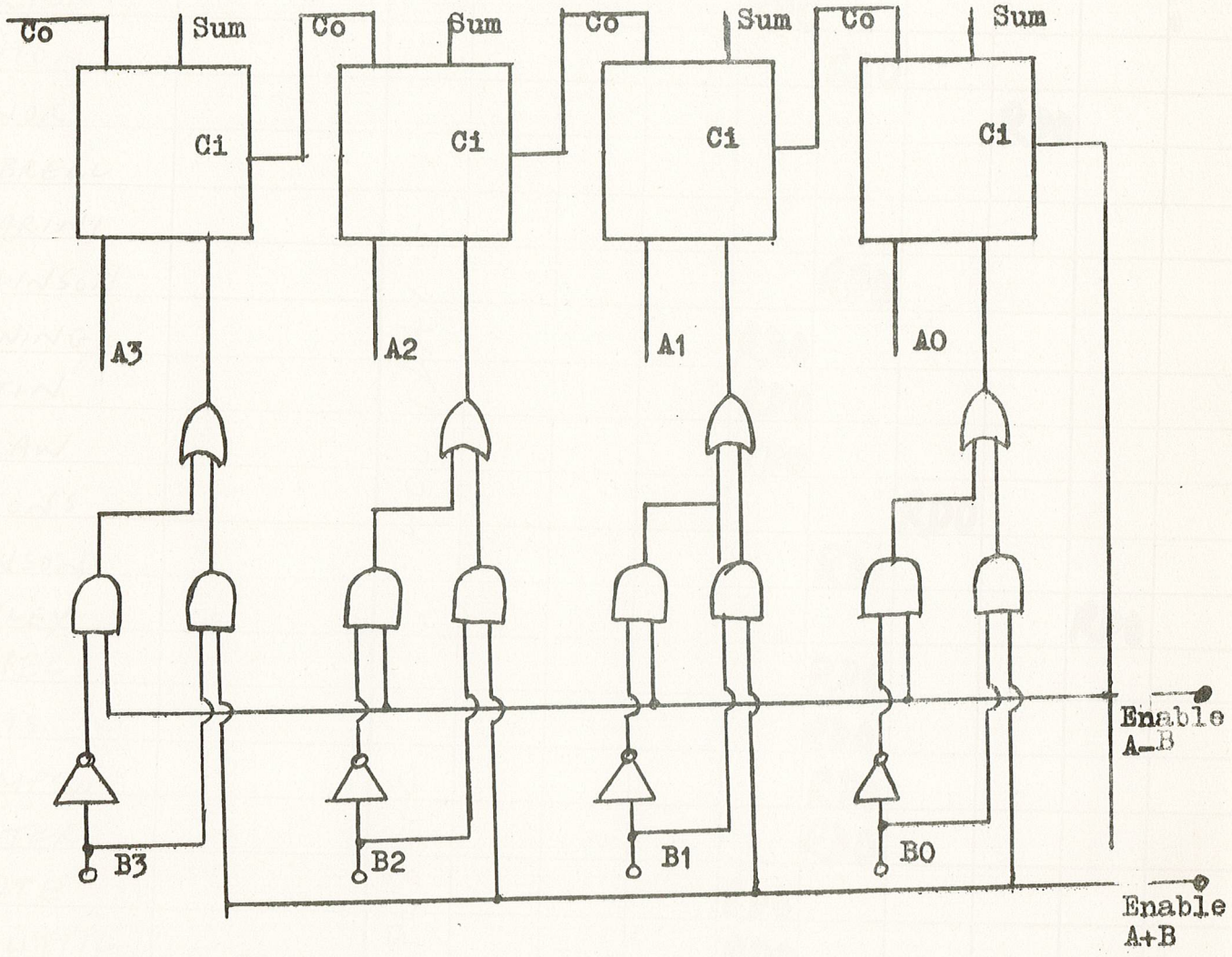


SElect Code			Function Done by ALU
S2	S1	S0	
0	0	0	Fn=0
0	0	1	Fn=An OR Bn
0	1	0	Fn=An.Bn
0	1	1	Fn=An⊕Bn
1	0	0	Fn=($\overline{An}$)+1
1	0	1	Fn=($\overline{Bn}$)+1
1	1	0	Fn=(An)+1
1	1	1	Fn=An+$\overline{Bn}$+Cn-1

4BIT PROGAMMABLE ARITHMETIC-LOGIC UNIT (ALU)

Operations performed by the ALU above as per the table are controlled by the states on the S leads or (functions select leads). As there are three bits of control information there are eight combinations available.

Parallel adder to perform addition and subtraction.



The adder drawn above shows the basic configeration used to add or subtract two four bit numbers.

To add, a one is placed on the A + B enable and the AND gates allowing the number to be fed in are opened. To subtract a 1 is placed on the A-B enable this opens the AND gates allowing the inverted number through to the adder. In addition this 1 is extended through to the carry in of the least significant bit adder. This has the effect of providing the two's complement to the adder.

MEMORY DEVICES

9.1 INTRODUCTION

The memory of a computer plays a very important role in storing information. This may vary from data we put in for processing, the processed data for future reference or the programme which tells the computer how to do its task.

Computer memories take many different forms, operate at a variety of speeds and depending on the type, find different applications in the same computer. Only some of the high speed versions are dealt within this Section.

9.2 MAGNETIC CORE MEMORY

In this type of memory the information is stored in minute RINGS or TOROID shaped sections of ferrite material. One bit of information can be stored on each toroid by magnetising the toroid core electrically in one direction or the other. Many thousands or in some cases even millions of toroids may go to make up a complete computer memory system. Each toroid shaped core is typically 5mm outer diameter for early memories but down to 0.5mm for modern memories.

The toroid cores are designed to have a square hysteresis loop, thereby retaining almost all of the saturation level of magnetism. Also toroids are very efficient, with very low losses due to leakage.

Information is stored on the cores by magnetising the cores in one direction or the other. In figure 28 if we pass a pulse of current through a wire which passes through the core, we can see that the core becomes magnetised in one direction. When the current pulse is removed the core remains magnetised in this same direction. If we assume this to be the logic 1 direction then we can say that we have stored a logic 1 on this core. If we apply a current pulse in the opposite direction as in Figure 29 we can see that the direction of magnetic flux

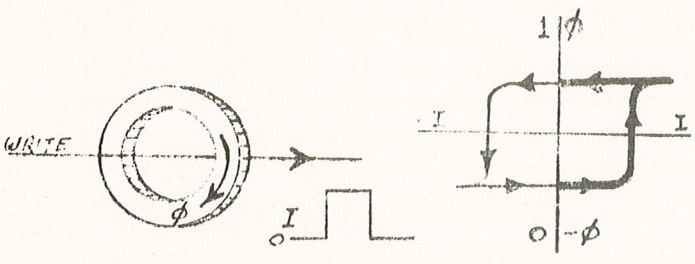


FIG. 28

will be reversed. We can now say that this core is storing a logic 0, and will "remember" this condition for long after the current pulse has been removed. To read from this memory, we pass another lead through the cores, as fig. 30 shows.

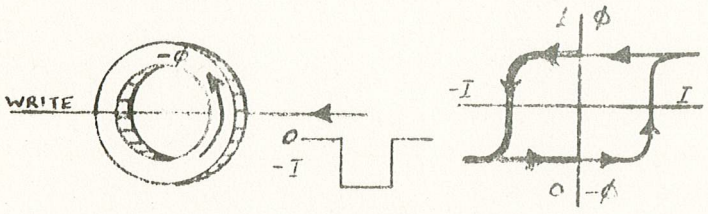


FIG. 29

To read information out of this core we pulse the write wire in the logic 0 direction. If the core had a logic 1 stored, then the flux direction would change and a voltage induced into the sense wire, indicating a logic 1. If a logic 0 was stored, then the flux direction would remain unaltered, and no voltage would be induced into the sense lead, indicating a logic 0. Note that when logic 1 was read the information stored in the core was altered. This is known as "DESTRUCTIVE READOUT" and after every read cycle we must have a write cycle to restore the information in the memory.

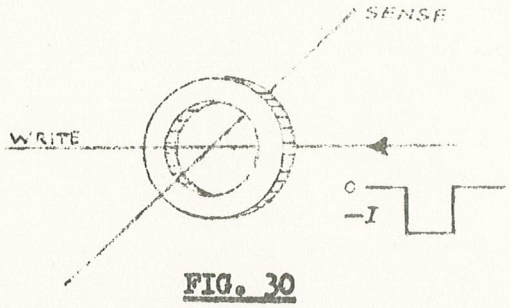


FIG. 30

Many thousands of these cores are used, side by side, in a computer memory. It would be impractical to have two wires per core in the memory. Because of this the sense wire may be common to all cores, and only the appropriate core is selected for reading, thus we know what is on any particular core we select.

Another way in which the amount of wiring is reduced is to use "half" write wires. Thus the amount of write wiring is twice the square root of the number of cores. (i.e. 10,000 cores, 200 write wires).

Figure 31 shows how the half write principle is applied. Assume the core to be magnetised in the logic 1 direction. If only one half write wire is pulsed in the logic 0 direction, then the magnetic field created is not strong enough to cause the flux within the core to change direction.

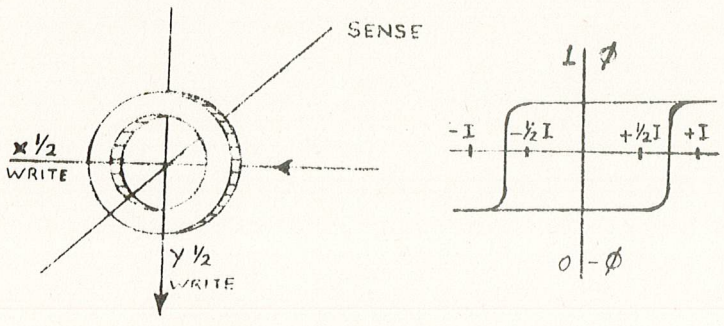


FIG. 31

If both half write wires are pulsed simultaneously, then the magnetic effect is additive and strong enough to cause the flux direction to change, thus causing the core to store a logic 0. This principle allows us to pass each half write wire through many cores, and only effect the particular core where the two pulsed wires cross. Figure 32 is a 16 core memory and the wires X2 and Y3 are pulsed. The only core effected is the one where these two wires cross (shown darker.) The other six cores are unaffected because the current in the half write wires is insufficient to have any effect on these cores. These memories are usually arranged in WORDS within the computer where a number of such memories are wired in parallel to form one word. The word is written in the memory on the identical core of each memory card. Thus a computer with a sixteen bit word would have sixteen such cards, all wired in parallel. To avoid writing the same information on all sixteen cores that form one word, an inhibit wire is used.

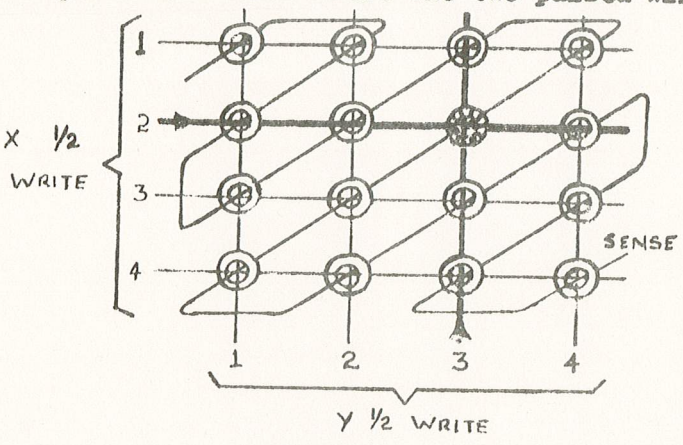


FIG. 32

Applying a ½ pulse of current on the inhibit wire in the opposite direction to the ½ write wires causes a cancelling effect and therefore the core is unaffected. Figure 33 demonstrates the inhibit principle. In this diagram the X and Y half writes are pulsed in the logic 1 direction. The inhibit lead is pulsed in the opposite direction with the same current magnitude of one of the half write wires. The net result is that only one of the half write currents is seen by the core, and this has no effect, on the cores flux.

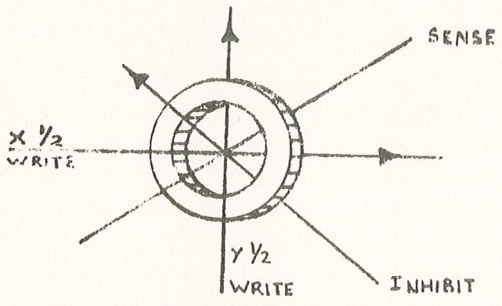


FIG. 33

Figure 34 shows how a four bit word is written into memory using the ½ writes and inhibit wires. If we assume that a logic 1 on the inhibit is no current and logic 0 on the inhibit is an inhibit current then we can see from figure 34 that only the cores on the first and last memory cards will have a logic 1 written into them. The cores in the two centre cards remain unchanged. It should be obvious by this that all cores for this word would have had to be set to logic 0 before this word was written into the memory. A complete write cycle, would therefore consist of selecting the appropriate X and Y wires, and doing a "READ".

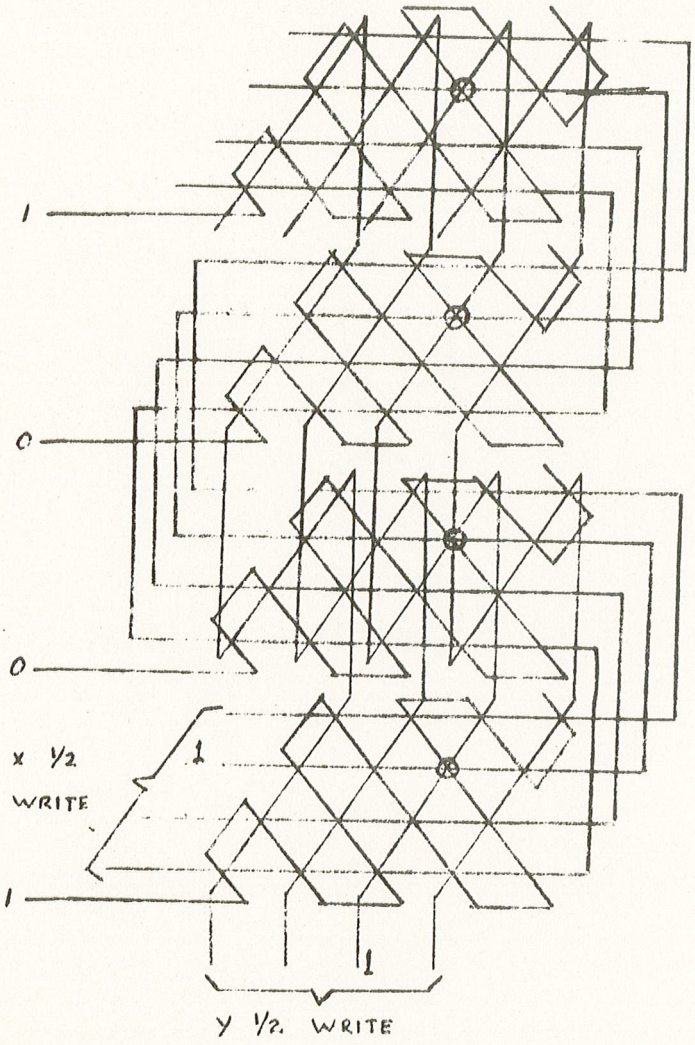


FIG. 34

This sets all the cores to logic zero, and the output as seen on the sense wires is ignored. Then the appropriate inhibit wires are selected, and the selected X and Y wires, together with these inhibit wires are pulsed simultaneously. This WRITES a logic 1 into the cores that only had the X and Y wires pulsed and leaves the cores that had all three (i.e. X, Y and inhibit) wires pulsed at logic 0. This completes the write cycle.

To read from the memory, the appropriate X and Y wires are pulsed in the logic 0 direction. This generates a voltage pulse on the sense wires that passed through a core which had a logic 1 stored. No voltage is generated on the sense wires which passed through a core storing logic 0. In the example of figure 34 a logic 1 would only be read out of the first and fourth plane of memory.

This voltage pulse read out is only present for a matter of nano-seconds. To make use of such a short pulse would be difficult. Therefore these pulses are stored on flip flops (Bi-stables) until the next pulse is read out. The information on the bi-stable is then used to re-write the information back into memory. In figure 35 we can see that if we pulse the X and Y wires to logic 0, and the core was storing 0, then a voltage would appear on the sense wire. This voltage is amplified by amplifier A, and a logic 1 put onto the D input of the flip flop.

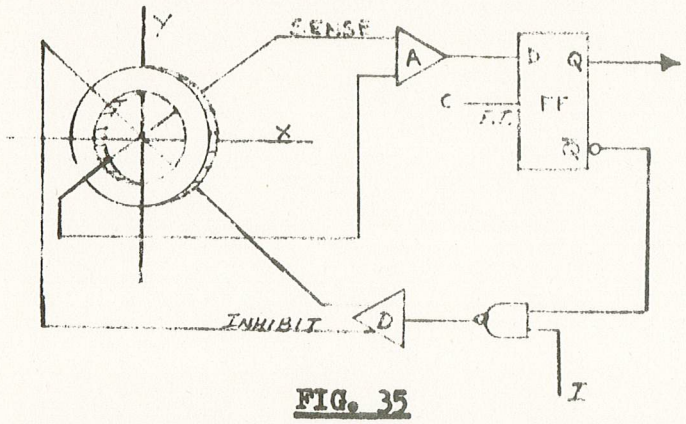


FIG. 35

The flip flop is then clocked, and the logic 1 appears on the Q terminal, to be used by the computer. Also to re-write the information back into memory, the X and Y wires are pulsed to logic 1 together with the I wire. As the $\bar{Q}$ terminal of the flip flop is at logic 0, the NAND gate output is logic 1 and no inhibit current is delivered by the Driver D. Thus a logic 1 is written back into the core.

If however, in figure 35 we pulsed the X and Y wires to logic 0 and the core was already storing logic 0, then no voltage would be induced into the SENSE wire and the output of the Amplifier A would be logic 0. When we clocked the flip flop, a logic 0 would appear on its Q terminal, to be used by the computer. The X and Y terminals are now pulsed in the logic 1 direction together with the I terminal. A logic 0 would therefore appear at the NAND gate O/P and the Driver D, would deliver an inhibit current. The core therefore remains in the logic 0 condition.

Notice that during the RE-WRITE cycles the flip flop was not clocked. This is to avoid any false transfer of information while re-writing into the memory.

9.3 THE ACTUAL CONSTRUCTION

The early types of core memories consisted of large number of cores, held in place and suspended by the four wires. With modern trends in minuterisation, this method is no longer favoured. The cores are therefore bonded to a copper covered fiberglass board. The copper acting as a shield against noise, and is shown in figure 36. As the hole in modern cores is less than 0.3mm in diameter only three wires are used. One is the X half write, the second is the Y half write and the third is used as a sense wire while reading and as the inhibit wire while writing.

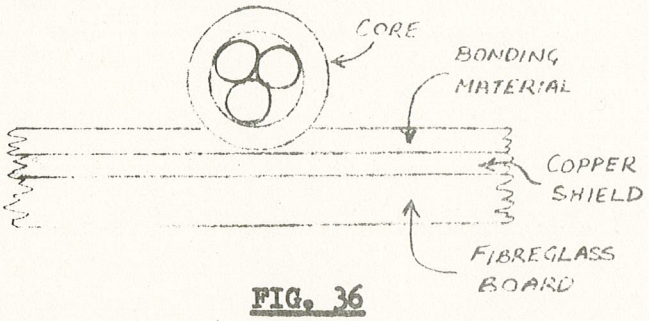


FIG. 36

If we consider a memory system capable of storing 32,400 words we would require 180 X wires and 180 Y wires and a total of 360 bi-directional current drivers (one for each X wire and one for each Y wire). This is a large number of drivers, even in integrated circuit form. Figure 37 shows how the number of drivers can be reduced from 360 to 20 by using 36 switches. Note that only the Y wires are shown for clarity.

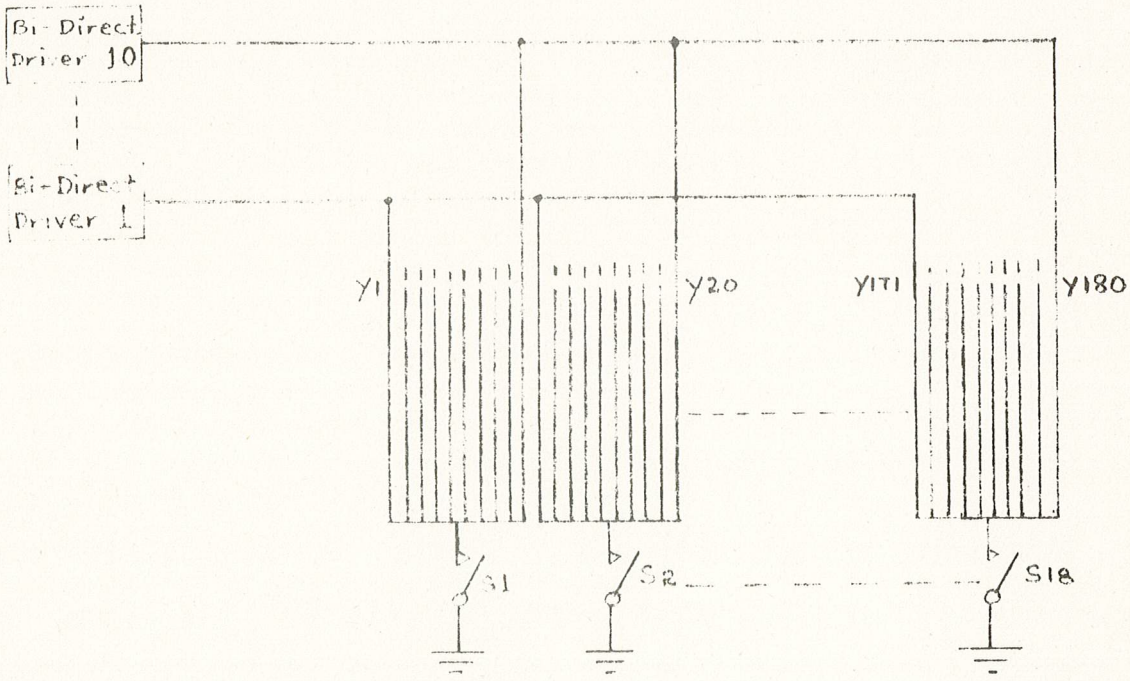


FIG. 37

The same applies to the X wires. In figure 37, if wire Y 20 was to be pulsed, we would energise Bi-Directional Driver 10 and close switch S2.

This would ensure that only wire Y 20 received a half pulse of current. By the same reasoning if we energised Driver 1 and closed switch S18 then only wire Y 171 would receive a half pulse of current.

We now have only 10 Bi-Directional current drivers for the Y wires and 10 for the X wires. We then have 18 solid state switches for the X wires and 18 for the Y wires.

9.4 CONCLUSION

Magnetic core memories have withstood the test of time and only at the time of writing (1977) they appear to be facing competition from solid state memories.

Advantages of Core Memories

(i) Non Volatile - Information not lost in case of power failure.

(ii) High Speed - Access to any word in 1μS. Complete read write cycle in 2μS.

(iii) Parallel readout of words.

(iv) Fairly compact - Modern 32K memory with support gear occupies approx. 400mm x 300mm x 10mm.

Disadvantages of Core Memories

(i) Requires Pos. and Neg. supplies - for the Bi-directional current drivers.

(ii) Requires large currents - Typically from 0.5 to 1 Amp. for half current pulses.

(iii) Good supply regulation - To ensure that cores switch correctly.

9.5 SOLID STATE MEMORIES

As solid state technology is constantly improving, so, larger memories are put into smaller chips at lower cost. At the time of writing (MID 1977), Solid State memories are used in approximately half the computers produced as the main memory. They are produced in most logic families and many are compatible between families.

9.6 TYPES OF SOLID STATE MEMORIES

Random Access Memories (RAM) or sometimes called Read and Write RAM (RAWRAM) is the solid state equivalent of the Magnetic Cone Memory. Its features are however, somewhat different as will be discussed later. Note, however, that if power fails, the data is lost - this is known as "VOLATILE."

Read Only Memories (ROM) these memories are PERMANENTLY written into by the manufacturer. The information they contain is NOT erasable. They are used mainly for "look-up tables" and "code converters." i.e. For a code going in, a different code comes out These memories are "NON VOLATILE."

Programable Read Only Memories (PROM) these memories are generally similar to ROM's but are programmed by the consumer. Once programmed they hold their information indefinitely.

9.7 BI-POLAR RAMS

In these memories the information is stored on flip flops made up of resistors and transistors. The power consumption of this type of memory is quite high (typ 6mW/Bit for standard TTL and 2mW/Bit for low power TTL) and because of this only small memories are possible. Maximum sizes are 64 bits for standard TTL and 128 bits for low power TTL. These memories are very fast however, with a typical access time of only 20nS. Figure 38 shows one memory cell of a bi-polar RAM. In this circuit, when the "Write Enable" lead is at logic 0, the output of the Tri-State gate TS is at + 1.5V. When the write enable lead is at logic 1, the output of TS is the same logic level as its input. Hence the name TRI-STATE for this type of gate.

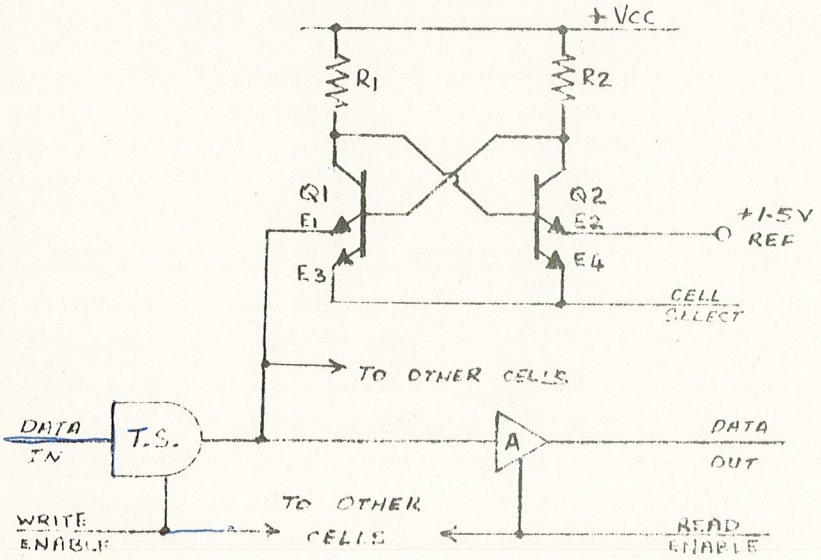


FIG. 38

To write into this cell the cell select line is taken to logic 1 (>2V) this causes emitters E3 and E4 to become reverse biased and lose control, while E1 and E2 become forward biased and gain control of transistors Q1 and Q2. The desired data is then applied to the "Data In" lead. At this stage the output of TS is still at +1.5V. When the "Write Enable" lead is taken to logic 1, then the "Data In" logic level is transferred to E1. If the "Data In" signal was logic 1, then E1 will be at logic 1 and Q1 will turn off. This causes base current via R1 to the base of Q2 and Q2 will turn on via E2 to the 1.5V REF. If "Data In" was at logic 0 then Q1 would be turned on via E1. This causes Q2 to turn off, due to Base E2 junction being reverse biased.

To store the information, the "cell select" lead is taken back to logic 0. This transfers control of Q1 and Q2 from E1 and E2 to E3 and E4 without upsetting the conditions of Q1 and Q2. The "Write Enable" lead can then be taken back to logic 0. The cell is now storing the data that was put on the "Data In" lead regardless of what condition is put on that lead now.

To read from this cell the cell select lead is taken to logic 1, transferring control of Q1 and Q2 back to E1 and E2. The "Read Enable" lead is then taken to logic 1. The Sense Amplifier A detects the condition of Q1 by sensing its E1 current. If a logic 0 had been written into this cell, Q1 would be off, no E1 current would be detected by the Sense Amplifier A and it would give a logic 0 output. Note that although a logic 1 was written in, a logic 0 was read out.

9.8 MOS RAM's

Only N channel MOS devices (N MOS) will be discussed as P channel MOS (P MOS) is now obsolete. Both types are identical in operation except for the reversal of supply voltages and logic conventions. The two differ however in their timing and power characteristics. N MOS being the more favourable.

These memories use only enhancement type MOSFET's and make use of all the Bi-Directional switching capabilities (able to conduct in both directions) of the MOSFET's. As MOS devices can be made to consume very low power, large memories are available on a single MOS chip.

At present memories with capacities of 4096 bits are quite common in STATIC memories and up to 16384 bits are being produced in DYNAMIC memories.

The size of MOS memories is not limited by the power consumption of the chip, as are bi polar memories, but by the number of devices which can actually be manufactured on a chip. These memories are slower than bi polar types with a typical access time of 400nS.

Static NMOS RAM

Figure 39 is the circuit to a static NMOS RAM. Q3 and Q4 act as load resistors. Q1 and Q2 are the active storage devices while Q5 and Q6 are the Bi-Directional input and output devices. The read data line is connected to a Sense Amplifier (not shown) and the Write Data lead is normally left floating until a logic level is ready to be written in. To write into this cell the Bit Select line is taken to logic 1. This turns Q5 and Q6 on. The appropriate logic level is then applied to the Write Data lead. Assume this to be a logic 1,

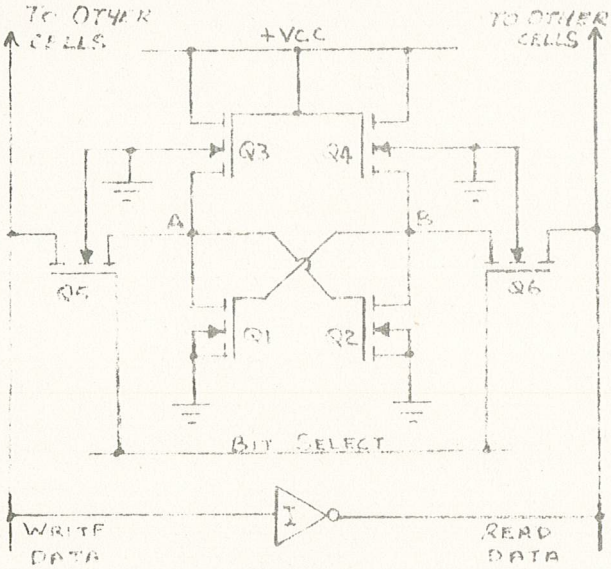


FIG. 39

this is extended to Q2 gate via Q5, and turns Q2 on. At the same time the logic level on the Write Data lead is inverted by I and applied to Q1 gate as a logic 0 via Q6 and turns Q1 off. At this stage a logic 1 is seen at A while a logic 0 is seen at B. The Bit Select lead can then be taken back to logic 0 turning Q5 and Q6 off, without disturbing the logic levels stored in the cell.

To read information from the cell, the Write Data lead is first allowed to float. The Bit Select line is then taken to logic 1, again turning Q5 and Q6 on. The logic level at A is passed through Q5 and inverter I to the Read Data lead while the logic level at B is read directly from the Read Data lead via Q6.

Note that for a logic 1 written into the cell, a logic 0 was read out.

DYNAMIC NMOS RAM's

Unlike the previous type of Bi polar and NMOS static RAM's, the Dynamic RAMS only hold their information for about 2mS. Because of this they must constantly be "refreshed" (re-written) every 1 or 2mS otherwise the information is lost.

Figure 40 is the circuit to a Dynamic NMOS RAM. Note that this cell only employs half the MOS devices that did the STATIC MOS cell. Therefore much higher capacity memories are possible with this type of construction. The capacitor C in this cell is NOT a separate capacitor but is the Gate to Source capacitance of Q2.

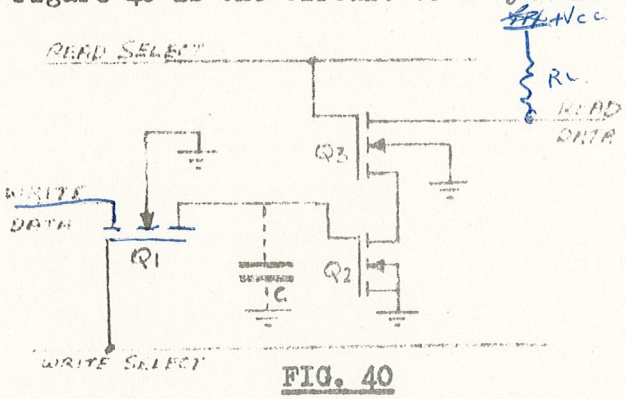


FIG. 40

To write into this cell the Write Select lead is first taken to logic 1, turning Q1 on. The desired logic level is then placed on the Write Data lead. If a logic 1 is placed on the Write Data lead then C will charge and if a logic 0 is placed on this lead then C will discharge. The Write Selected lead is then taken back to logic 0 turning Q1 off and isolating C from the Write data lead. To read from the cell the Read Select line is taken to logic 1, this turns Q3 on. If a logic 1 had been written into the cell, C would be charged holding Q2 on and a logic 0 would be seen at the Read Data line. If a logic 0 had been written in, then C would be discharged, holding Q2 off. When Q3 turns on, this would be read as a logic 1. Note once again that for a logic 0 written in, a logic 1 was read out.

Another type of NMOS RAM also exists. It consists of a single MOSFET and a separate Capacitor C as shown in Figure 41. Due to the simplicity of this type of cell, memories with up to 16384 bits are now being produced on a single chip. Up to 65536 bits are expected on a single chip by 1979. To write into this cell, the Select line is first taken to logic 1 turning Q1 on. The desired logic level is then placed on the Data

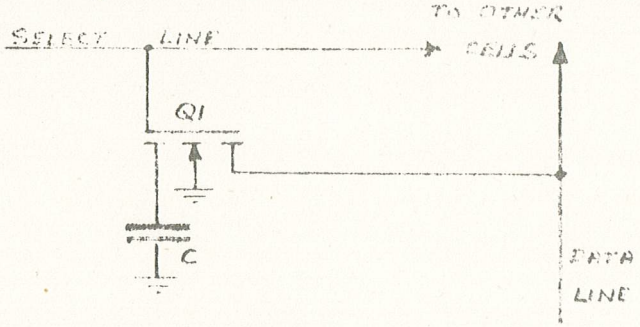


FIG. 41

Line. A logic 1 causing C to charge and a logic 0 causing C to discharge. The select line can then be taken back to logic 0, turning Q1 off and isolating the capacitor from the Data Line. To read from the cell, the Select Line is taken to logic 1 turning Q1 on and the Data Line sensed, via a Sense Amplifier. A charge on C giving logic 1 out and no charge on C giving a logic 0 out.

As mentioned before, Dynamic RAMS only hold their information for as long as the capacitor remains charged. This is only a few milli-seconds. A refresh circuit must therefore be employed which reads each cell in turn and re-writes this information back into the cell, in order to store the information for long periods.

9.9 READ ONLY MEMORIES (ROMS)

Once these memories have been written into, the information cannot be altered. They are known as "Mask Programable" and the information is written into them during manufacture, by a photographic "Mask" which specifies the state of the memory cells by determining which cells are ON and which cells are OFF.

The customer can specify his own program to be written into a ROM but as the MASK are quite expensive to produce, costing around $4,000 each, it is not economically feasible to order a ROM unless great numbers of them are required. Some of the more popular functions are already pre-programmed by the manufacturer and these retail for between $5 - $50 depending on complexity and demand. Typical examples of what is available "over the counter" are:-

BAUDOT CODE TO ASC 11 CODE CONVERTER
SIN LOOK-UP TABLE
BINARY TO SEVEN SEGMENT DECODER

9.10 PROGRAMABLE READ ONLY MEMORIES (PROM's)

These are basically the same as MROM's except that they are programmed (written into) after manufacture instead of during. Again, once written, the information cannot be erased. Figure 42 shows a small portion of a PROM. The PROM is manufactured with all the "Fusible" diodes in place. The memory is programmed by "blowing" the unwanted fuses, thus effectively open circuiting the diodes. If fuse D1 was blown and D2 left in tact, then when Address line A is made logic 0, Data line C will be logic 1 and Data line D logic 0 (due to D1 open cct and D2 conducting). These memories can be programmed by the consumer on a special programming tool, which contains a socket for the I.C., a set of switches on which the Address is set up and a set of switches on which the required Data out is set up. A "Write" button is provided, which when pressed passes sufficient current through the unwanted diodes to "blow" them. However, if the programmer makes an error, the PROM must be discarded. The manufacturer will also program these PROM's to customer specifications for an additional charge.

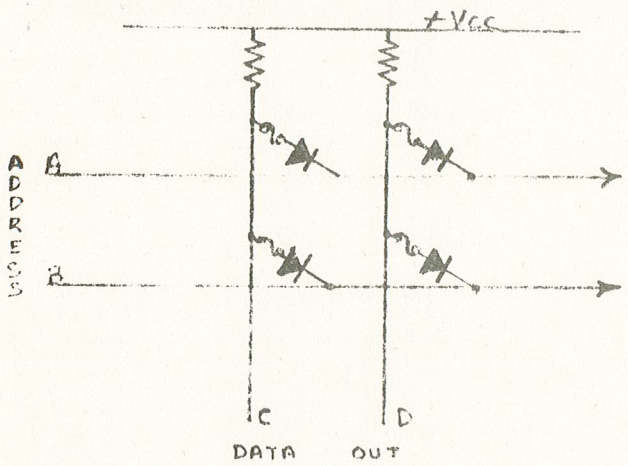


FIG. 42

9.11 ERASABLE PROGRAMABLE READ ONLY MEMORIES (EPROM's)

These types of memories are sometimes called Re-programable Read Only Memories (RPROM) or Read Mostly Memories (RMM). They are MOS memories and are easily identified by a clear quartz window on top of the I.C., package through which the chip can be seen. They are programmed in a similar way to PROMS, but the programme is stored on a "permanently" charged cell, by shifting the energy level of the semi-conductor material. The change stored takes about 10 years to leak away, after which the memory must be re-programmed. If, however, the quartz window is exposed to Short Wave Ultra-violet light the charge leaks away in a matter of seconds. The memory can then be electrically re-programmed.

9.12 TYPICAL MEMORY ORGANISATION

Memories are organised with a number of "Address" lines, which select the memory location, one or more Data lines from which data can be read and one or more Input lines on which data to be stored can be put into the memory. Some memories use bi-directional data lines. i.e. the same lead for input and for output

Address Lines

These leads are "binary weighted" so that a memory with 4 address lines, contains 6 memory locations, one with 6 address lines has 64 locations, one with 8 address lines has 256 locations and so on. Each memory location or address may only contain one bit or may contain several bits.

Input and Output Lines

These may either be separate or the same pins on the I.C. depending on the type of memory. These may be organised as single bits. Such a memory would only have one lead available for Input and Output. An example of this is a 64 x 1 memory shown in Figure 42. This memory can store 64 bits and each address stores 1 bit. Another type of memory is organised in "word" form. This type has one Input and Output pin for every bit in the word. A word can consist, generally of 4, 8, 12 or 16 bits. An example of this type of memory is shown in Figure 43. This memory is a 16 x 4, it can also store 64 bits but they are organised in 4 bit words. Everytime a location is addressed, 4 bits are read out simultaneously.

Both memories shown in Figures 42 and 43 are RAMS. Only one type of each RAM is demonstrated here and other versions exist. ROMS and PROMS use the same type of layout, but have no Input Data leads.

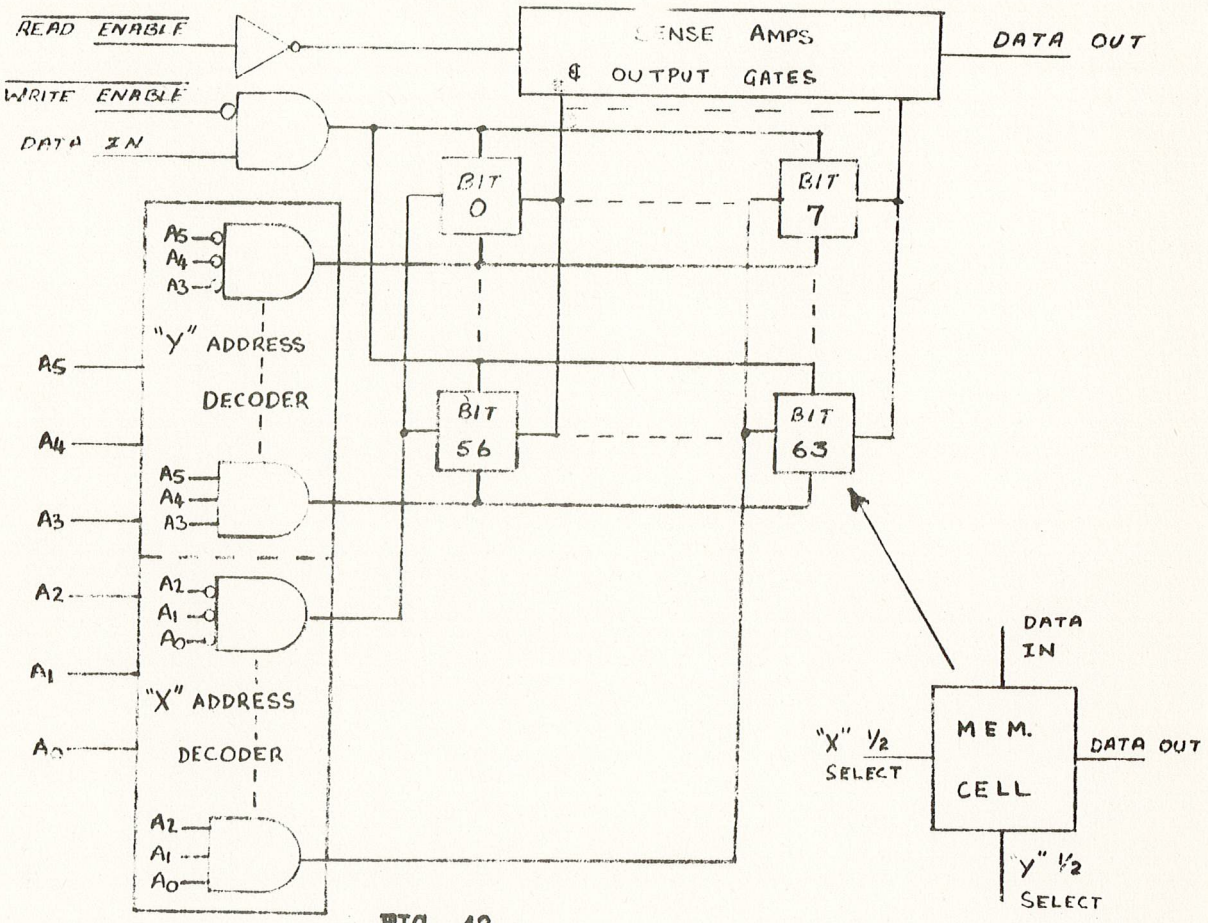

READ ENABLE
WRITE ENABLE
DATA IN
SENSE AMPS
& OUTPUT GATES
DATA OUT
BIT 0
BIT 7
BIT 56
BIT 63
A5
A4
A3
"Y" ADDRESS
DECODER
A2
A1
A0
"X" ADDRESS
DECODER
DATA IN
"X" ½ SELECT
MEM. CELL
DATA OUT
"Y" ½ SELECT

FIG. 42

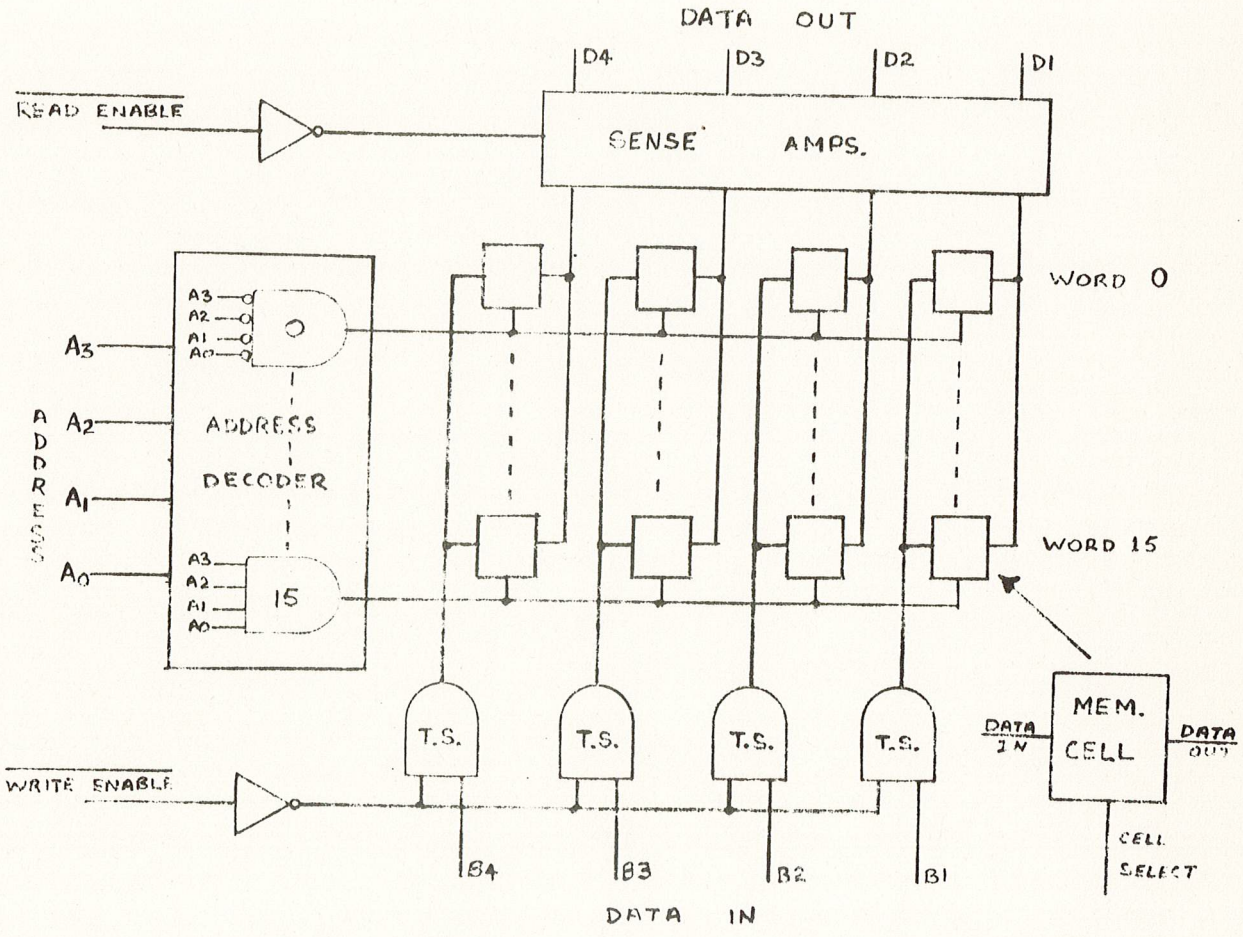

DATA OUT
D4
D3
D2
D1
READ ENABLE
SENSE AMPS.
WORD 0
WORD 15
A3
A2
A1
A0
ADDRESS
DECODER
T.S.
MEM. CELL
DATA IN
DATA OUT
CELL SELECT
WRITE ENABLE
B4
B3
B2
B1
DATA IN

FIG. 43

9.13 CONCLUSION

Solid state memories in their many forms are speedily replacing Magnetic Core Memories. By 1980 it is expected that all computers produced will use Solid State memories as their main memory system. At present a 16k (16384) bit solid state memory costs 0.08 cents per bit. This is about 10% of the cost of a similiar size Magnetic core memory.

Advantages of Solid State Memories

- Economy (Except ROMs in small quantities)
- Compactness
- Reliability
- Versatility
- Speed

Disadvantages of Solid State Memories

- Volatile (RAMS only)
- Constant power drain

Section 10

Input/Output Devices

Since most pieces of equipment used with computers are capable of providing data to the computer and also of reading it from the computer, input/output equipment will be considered as one topic. For the computer user the input/output pieces of equipment are the most important. They enable him to handle his data in the most efficient and expeditious manner. The computer proper is merely a high speed calculator performing many calculations per second. It is the input/output equipment that is usually of most concern to the user.

In the simplest terms, input equipment consists of pieces that provide binary or binary coded data for use in the computer and output equipment consists of those that accept binary or binary coded data from the computer for outside handling or storage.

Control of the input/output equipment may be in the central computer itself, in the specific piece of equipment or in both. When one or two units are operated the central computer will provide timing signals that determine when to start feeding data, what data to use, and when to stop. Since the input/output units are the slowest operating of a computer system, the intergrations of many different pieces of equipment is necessary to provide the computer arithmetic unit with sufficient data to operate continuously.

It is possible for one central computer unit to have a dozen, magnetic tape and magnetic disc units providing input data to it while feeding data out to other magnetic tape, disc and high speed printer units.

Types of Input/Output Devices

High Speed Media = Machine Created

- Magnetic Tape — 96000 CHARACTERS PER SEC.
- Magnetic Disc — 66000 CHARACTERS PER SEC
- Cassette Tape — " " "
- Visual Display Unit — 4800 BITS PER SEC
- High Speed Line Printer —

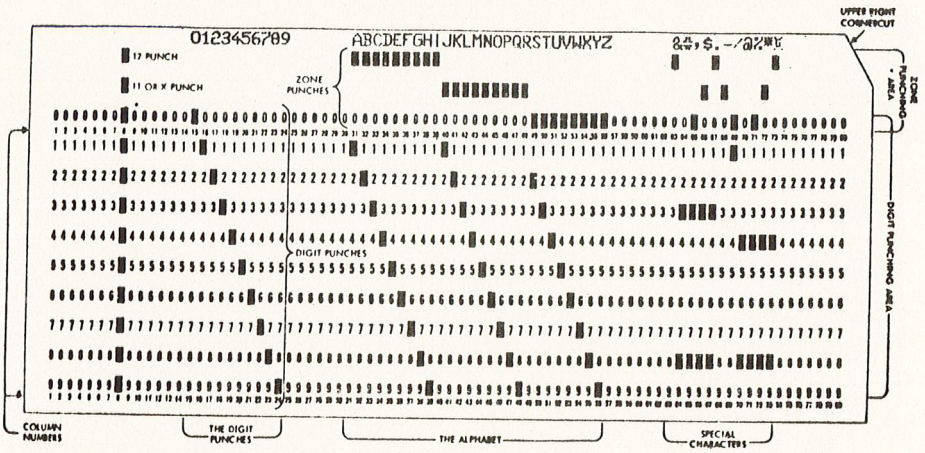
Slow Speed Media = Operator created

- Punched cards — 1000 CARDS PER MINUTE (200-250 CARDS PER HOUR CREATED.)
- Paper tape — 150 — 1500 CHARACTERS PER SEC.
- Tele - Typewriter — 10 CHARACTERS PER SECOND.

Punched Cards

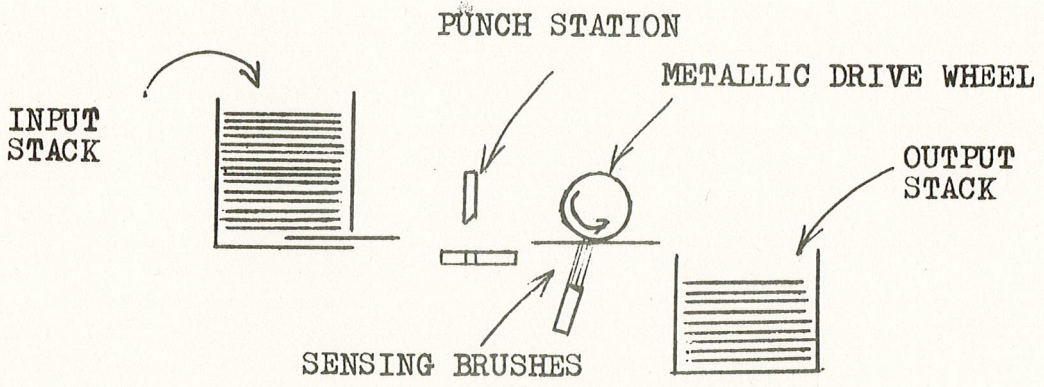
Punched card data processing provides a widely used method of feeding digital information to a computer. The card has a fixed layout and stores binary data in the form of punched out holes or no holes for 1 and 0 respectively. The data storage is of course permanent. A card can hold a small amount of data usually on a specific item. Its direct relationship with one item (It could be an individual student in a school or a specific item of manufacture such as a part of a car) is very useful when the ability to handle each card or each item separately is desirable if not necessary. When item of data is stored on one card, the cards can be separated by item using a card sorting machine. For a set of cards representing each student in the school, the cards can be sorted by class, section or any other desirable breakdown for record purposes.

A standard card contains eighty columns and twelve rows. Each column can be used to represent a character. The data is coded using a simple code so that the cards are easily read by an operator. See card below.



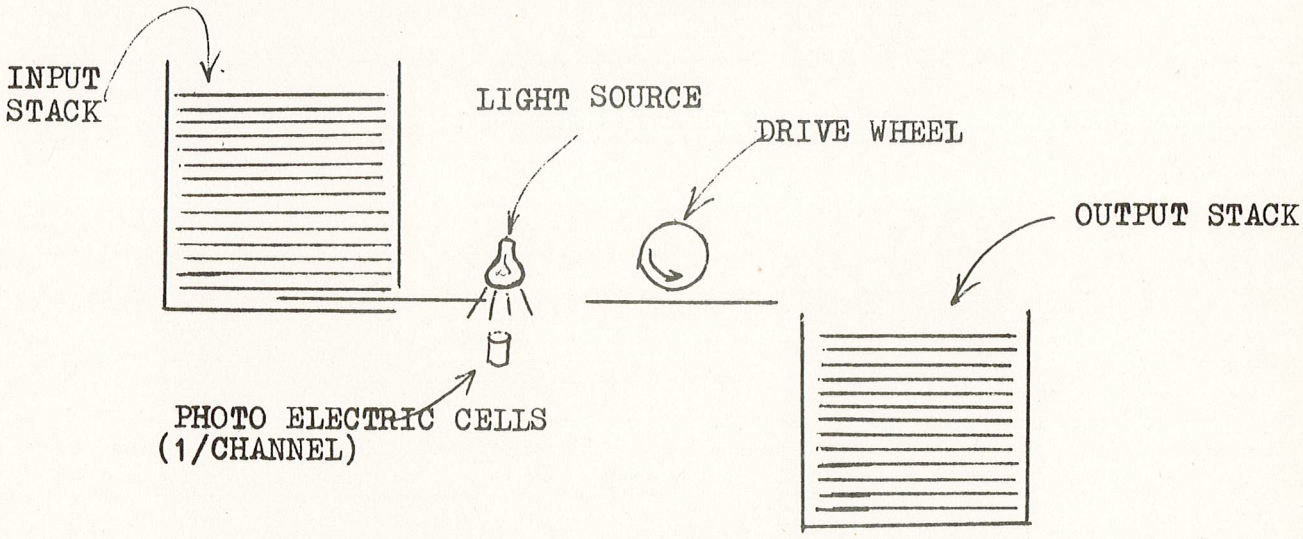
Standard Hollerith Code used for punched cards.

Punched cards are handled surprisingly fast. Reading rates of over 1000 cards per minute are currently available. Punching rates very from 120 cards perminute to 250 per minute. There are two popular types of card reader units. The slower method uses wire brush sensors (see diagram below). If a brush goes over a hole it makes contact with a metal plate below and passes this on as a signal of binary 1 being read. The brush readers only operate up to rate of about 200 cards/minute.



CARD READER -- BRUSH SENSING.

The faster card reading rates mentioned previously are obtained using optical readers. A light source on one side of the card will activate a photo detector, if there is a hole to pass through (binary 1) and does not activate the detector when the card face is present. Since the optical cells respond quickly, the reading rate can be increased.



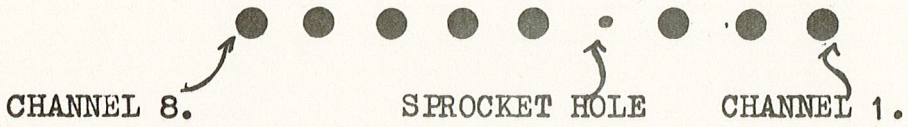
CARD READER --OPTICAL SENSING.

Control of the card reader is generally within the external unit, the computer only controls when to start reading. The data stored on many cards might be used to fill up part of the core memory. Once filled, the computer operates at high speed from the internal memory.

Punched cards may hold both program material and data for use in the computer. Recalling that the hardest part of the job may often be to provide data fast enough to keep the arithmetic section busy, you may find such combinations as punched cards feeding magnetic tape units which are then used to feed core memory.

Punched Paper Tape

This medium is commonly found in digital computer systems, mainly in the form of eight channel paper tape such as the following:

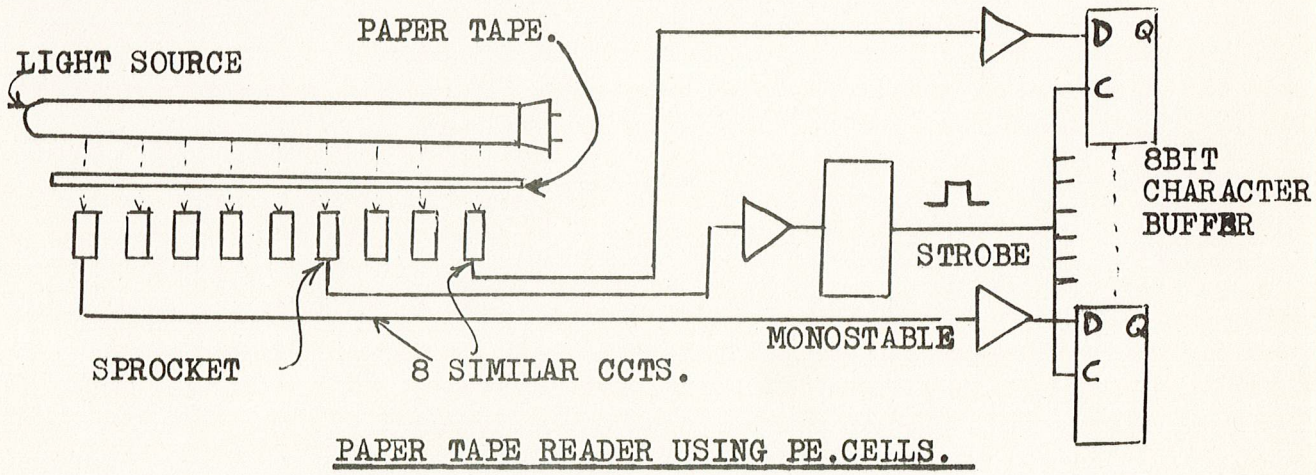


8 CHANNEL PAPER TAPE CONFIGURATION.

The information is punched in binary coded characters across the tape, three bits on one side of a smaller hole (called a sprocket hole) and five bits on the other side. A hole represents a binary "1" and no hole represents binary "0". The sprocket hole is used to provide binary information to the paper tape reader for synchronisation.

The alpha-numeric characers of a source program are usually punched in binary coded form onto the tape from a paper tape punch attached to a key board, such as a teletype. Different binary coded alpha-numeric codes are used but the ASCII Code (otherwise known as CCITT NO. 5) is becoming the universally used code.

The paper tape can then be read into the computer via a paper tape reader which a senses the information via photo-electric cells or mechanical brushes..



PAPER TAPE READER USING PE.CELLS.

The paper tape is fed through the reader at a controlled speed typically 150-1000 characters/sec. The photo-electric cell underneath the row of sprocket holes is used to trigger a stroke which samples the output of the other eight photo cells.

This eight bit character can then be latched into an eight bit character buffer (register), checked for correct parity and then stored in the computer (as determined by the computer programme and input unit).

If the information on the paper tape is binary coded alpha-numeric information (e.g. ASCII) then a programme is used to interpret this coded information. For example, if one has written a programme in assembly language, then a typical instruction such as LDA 3 and 6 would be input under control of the assembler programme, eight ASCII coded eight bit characters and the assembler programme would interpret these characters and then assemble one machine code instruction.

e.g. 0011101100000110. After the complete source "source programme" (assembly mnemonics) has been inputed and assembled the "bbjectprogramme" can be punched out from the computer in binary form via a paper tape punch. The information would now not be in the form of ASCII characters but instead would be in straight binary. Eight bits at a time punched across the tape e.g., the above machine code instruction would be punched across the tape as 00111011

00000110

sprocket

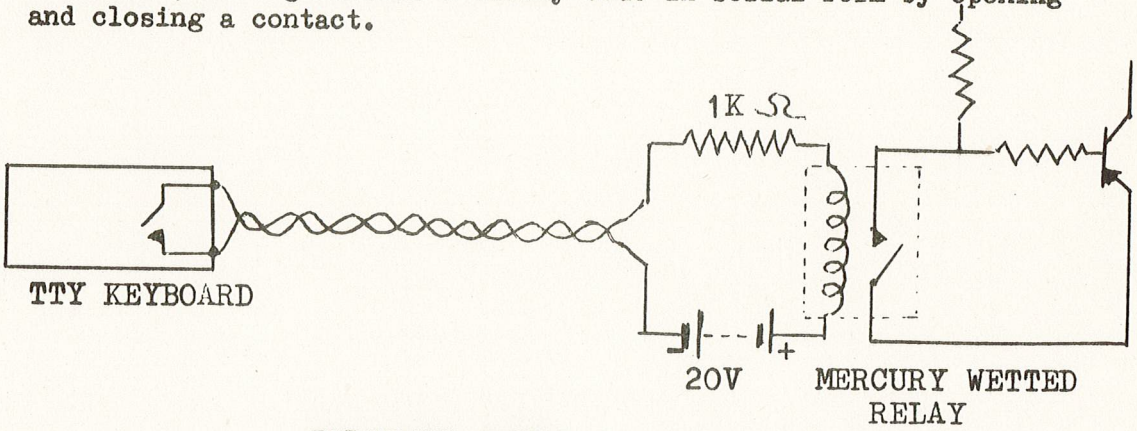
At some later time, the binary "object tape" could be loaded into the computer (by another programme called a "binary loader" not the "assembler programme") and run.

In summary, the information stored on paper tape could either be in the form of binary coded alphanumeric characters (ASCII) or as straight binary information.

Teletypewriter Input/Output

A commonly used I/O Device is the teletype.

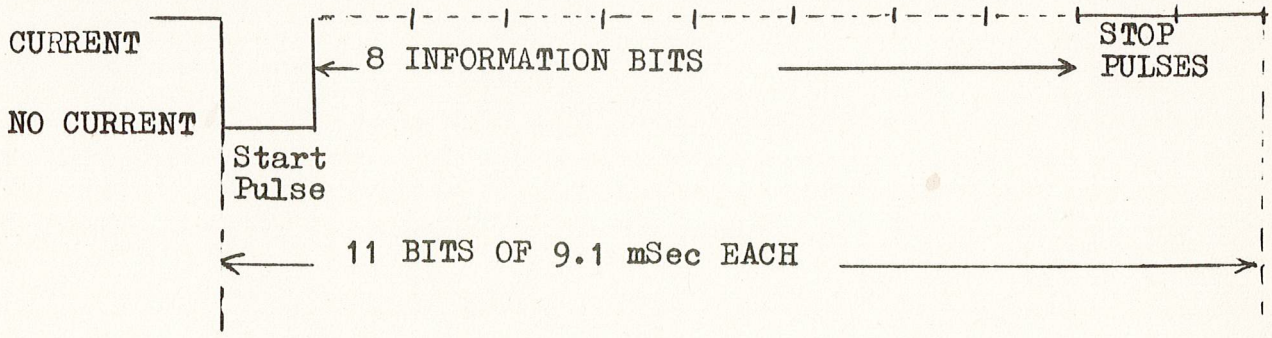
(a) The teletype input is actuated from a keyboard where a key is depressed for the respective alphanumeric character. Through a series of mechanics, this generates a binary code in serial form by opening and closing a contact.



TELETYPE INPUT.

In the rest condition, the contact is closed and therefore current flows in the twisted pair line. When a key is depressed on the keyboard, this current is interrupted such that a binary 0 corresponds to no current and a binary 1 corresponding to current. This current is used to operate a mercury wetted relay, the output of which is a clean signal (without noise from contact bounce of the original contact) which can operate some digital logic in the interface unit in the computer.

The teletype operates at a maximum speed of ten characters/second (i.e. 100 mS/ch) Each character is coded into a start bit, eight information bits, two stop bits.



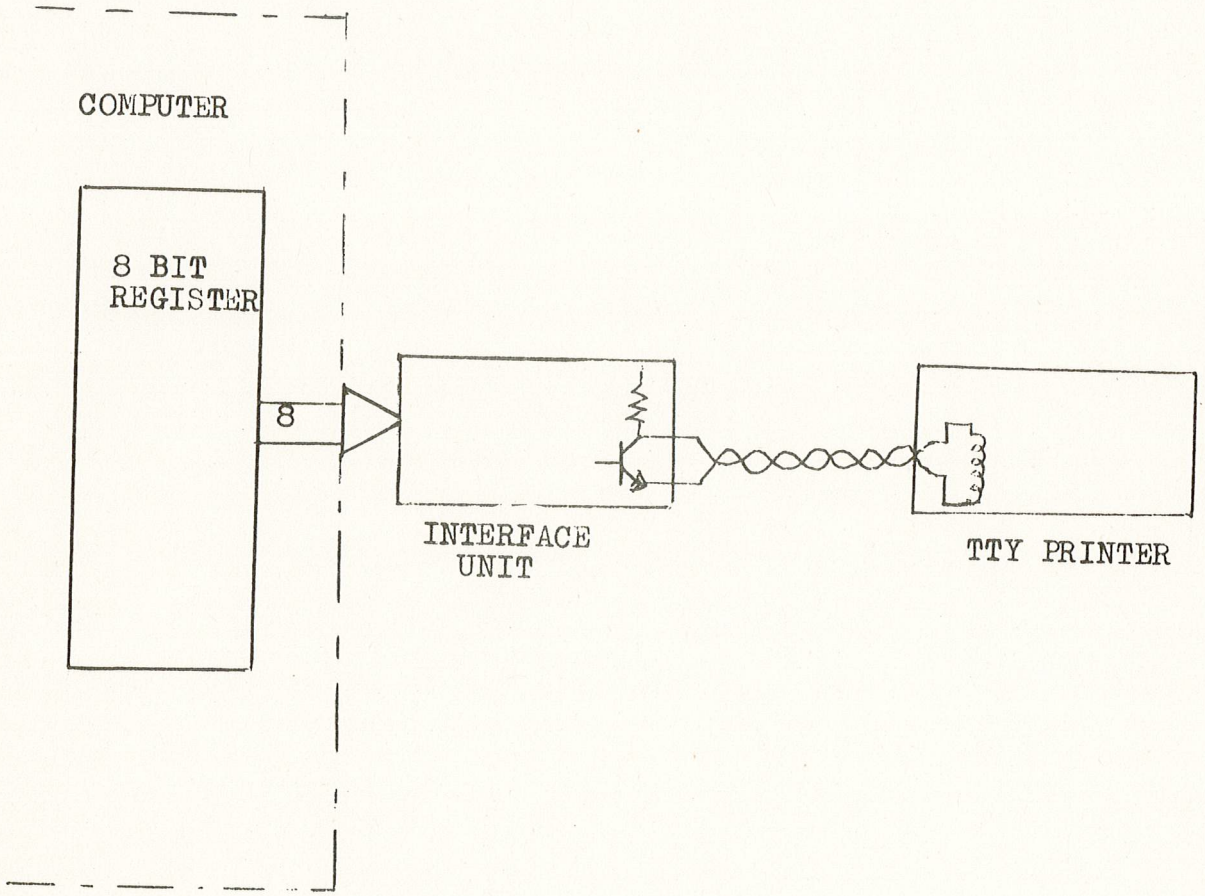
ELECTRICAL OUTPUT OF TELETYPE OR TELEPRINTER.

The speed of the teletype is limited so that the next start pulse cannot occur before the end of the second stop bit of the previous character; that is, minimum period between start pulses 100mS.

The start pulse is used to trigger a clock circuit which strobes the eight information bits at mid bit position.

The Teletype Output

Output from computer to teletype is achieved by sending on eight bit binary coded character from a register in the computer to a special shift register in an interface unit which perform the necessary parallel to serial conversion. This character is sent out in serial form (along with a start pulse and two stop pulses) to the teletype at a speed of 9.1mS per bit (100mS/CH). This is achieved by interrupting current in a twisted pair line which thereby operates the teletype printer.



TELETYPE OUTPUT CONFIGURATION.

Notice that two twisted pair lines are required between the teletype and the interface unit (one pair input, one pair output) but the interface unit requires logic to do the appropriate serial/parallel (input unit) and parallel to serial (output) conversion.

Magnetic Tape

Magnetic tape is a very important and widely used medium for storing digital information. It can either be classified as an input/output medium or as a method of providing bulk storage of information as a back up to the main memory within the computer.

Magnetic tape is convenient because it can store large amounts of data. It is also flexible and can readily be transferred from one machine to another thus enabling large amounts of data to be made available for data processing regardless of origin.

The tape itself consists of mylar, acetate or polyester base, 1.5 mhs thick, coated with ferromagnetic material mixed with a binder. The most commonly used tape widths are $\frac{1}{2}$", $\frac{3}{4}$" x 1" a typical size reel contains 2400 feet of tape.

Like paper tape, magnetic tape is divided lengthwise into channels. In these channels data is recorded in the form of magnetised spots. Each continuation of spots corresponds to a letter or a digit.

The data is written on magnetic tape in records with a gap separating them and the information is read or written on one record at a time. A record basically consists of a number of data words and may be of any length, although normally a maximum record size will be specified for ease of programming and control.

One widely used system consists of seven tracks (six data bits plus one parity bit) each track being about .03 inches wide and separated about .06 inches between centres. This means that one six bit binary coded character can be recorded across the width of a piece of $\frac{1}{2}$" tape. The information is read from the tape by a block of seven replay heads which must be accurately aligned. Recording onto the tape is achieved by a block of recording heads with similar critical alignment.

The tape is moved past the heads at a controlled speed of typically 100 inches/sec.

The packing density in the longitudinal direction is limited by the quality of the grain size of the magnetic material on the tape. Commonly found packing densities are 556 bits per inch and 800 bits/inch.

Example 2400 feet of magnetic tape ½" wide packing density = 800B.P.I.

Q. What is the maximum number of characters that can be stored on the tape?

Q If the tape moves over the leads at 100 inches/sec, then the transfer rate is?

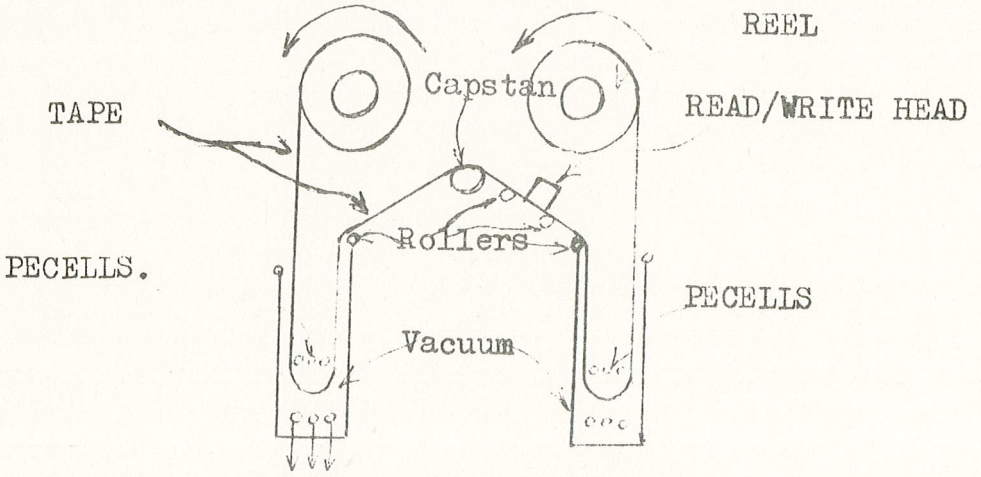
The reel of magnetic tape is mounted into a transport which controls the movement, reading and writing of the tape. This transport also contains the required electronics to interface the unit to the computer input/output bus. Thus the magnetic tape unit is a major component in a computer system that makes available valuable data, documents or large files of information accessible to the computer at a high speed.

The transport is much more expensive than a paper tape reader and punch. It is also impossible to visually send the data as one can do with cards. Also is it essentially a "sequential access memory" rather than "random access".

Example If the required information begins half way down the tape, then it may require 144 seconds to gain access to this tape (100 IPS, 2400 feet tape reel).

Another advantage of magnetic tape is that data can be written on it, read back immediately; or at a later date, and even on a different transport. It can also be erased at any time and the same tape reused for storage of different data.

The operation of tape drives for both ½" x ¾" tape is as follows: magnetic tape may be read forward or backward, writing is achieved in a forward direction only. Data is read or written when the tape passes under the read/write heads. This is the only object which makes contact with the recording surface of the tape. Tape motion is achieved by applying vacuum through one of two capstans (one for forward, the other for reverse) which are continually rotated at a constant speed. Tape slack is vacuum controlled in vertical chamber.



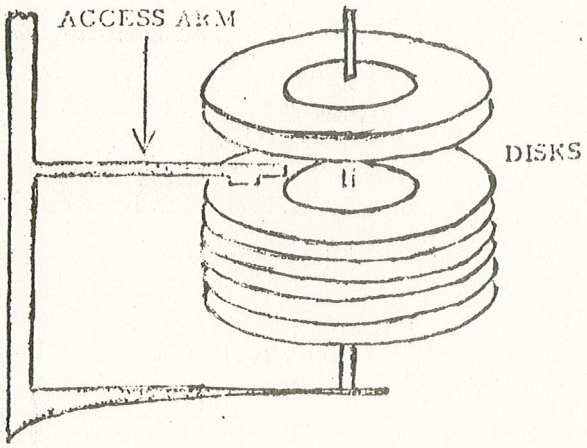
MAGNETIC TAPE CONSTRUCTION.

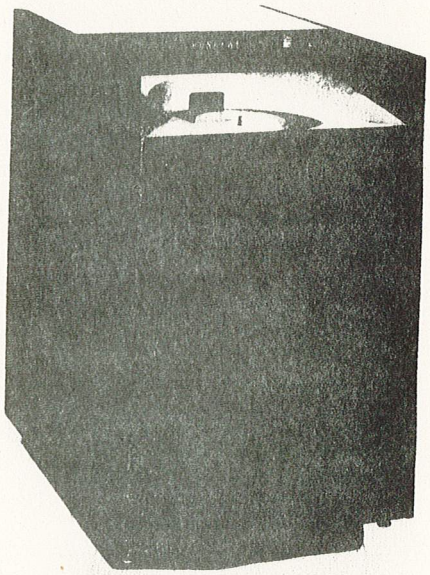
There is a fixed starting and finishing point on the tape reel. This ensures that data is always written and later read from the same starting position on the tape and finishes on the same position. This also allows for a portion of tape at either end be free for threading onto the tape reels. There starting and finishing points are detectable by the drive mechanism.

As a summary, the magnetic tape can store up to 1600 characters per inch, or tens of millions of characters on a 2400 feet reel of tape. Storage is sequential, in blocks or records and is erasable. It is cheap storage per bit but expensive for millions of characters. The magnetic tape unit has large storage capacity but long access time. Magnetic tape can be used or classified as being both bulk storage or as an input/output device.

Magnetic Disc

A common feature in modern computers is that disc storage may be provided in removable self contained packs giving virtually a limited storage capacity.





Magnetic discs may be used for both bulk storage or an input/output device as for magnetic tape.

Magnetic disc storage consists of a number of thin metal discs coated on both sides with magnetic recording material, spinning about a central vertical shaft. Data is recorded as magnetised spots on magnetic tape, so that the method of construction and recording on the magnetic disc is the same as magnetic tape only the mechanics of reading, writing and driving will differ.

Each surface of each disc has a number of concentric recording tracks, also the surface is divided into equally sized sections known as sectors. The number of records in a magnetic disc storage device depends on:

* The number of discs
* The number of tracks on each disc
* The number of records on each track

Each recording surface may contain typically between 100 - 250 tracks. Disc diameter vary from 1 - 3 feet. The disc may be rotated at about 1800 revolutions per minute.

Considering the disc alone, the average access time would be about 50mS. However, there are many possible tracks and usually one head per surface. Adding in the time needed to move the read arm to the desired track brings the overall average access time around 250mS. Although this may seem a long time when compared to access time for magentic tape. (In the order of seconds) it is very fast.

The access arm has a lateral motion and has attached to it several read write heads are for each disc surface. Movement of the access arm can position the read/write leads in order to read data from a particular sector on a particular track on a particular disc surface. Each sector therefore has an "address" made up of identification of disc surface, track and sector.

The main feature of magnetic disc storage is that any location anywhere in the disc device can be assessed in approximately the same time as any other location.

There are two main forms of access to the file. One is Sequential processing in which records are read or written in sequence of address and the process therefore to all intents and purposes is the same as magnetic tape. The other form is random access processing. In this form some method is used to relate the identity of the record (the fields used to normally classify its sequence in the file) to disc address. Thus, the field data is not stored in address sequence. When transactions are processed, the same method is used to find the master record as was originally used to store it. The advantage of this system is that it is only necessary to process those master records, that are affected and no reading of master records takes place with no transaction record.

Another dissimilarity is that the updated record may be written back onto the same disc in the place from which it was read. This obviously replaces the previous information that was there so that at any time the record reflects the latestinformation.

Commonly used types of removable discs at present are:

1. Single platter cartridge - two surfaces

2. Six platter disc pack - 10 surfaces

3. Eleven platter disc pack - 20 surfaces

High Speed Printer

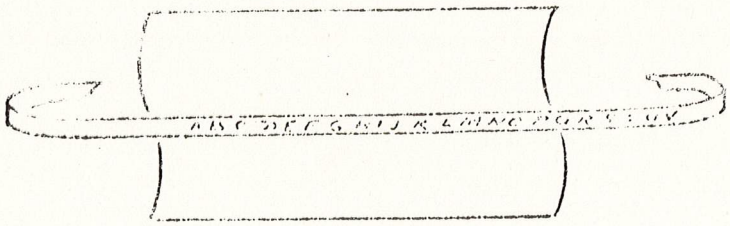
Printer listings form the final output of most computer programmes. Continuous stationery is mechanically fed through the printer under the control of the programme and characters are printed upon the paper by one of several means.

Bar Printer

This form of printer has separate print wheels or print bars. There are as many print bars/wheels as desired characters/line. Each print bar/wheel contains a complete set of alphanumeric characters and special characters. For the printing of each line, each wheel representing a character of the line must be rotated to the desired character. When all print wheels are in position, mechanically driven hammers (one for each character) are activated and strike the ribbon thereby printing all characters of the line at once. For each line of print the computer feeds in new data to the printer unit. After each line of print the paper and the ribbon are moved slightly and the print wheels or bars are moved to their new position and the hammer having moved off strike again for the next line of print. A printing rate of 200 lines per minute is typical for this type of unit.

Chain Printer or Belt Printer

This unit uses a continuously rotating belt, containing all the characters of the set. The individual hammer (one for each character position on the line) strike as the desired character on the belt passes underneath the hammer head.



CHAIN OR BELT PRINTER.

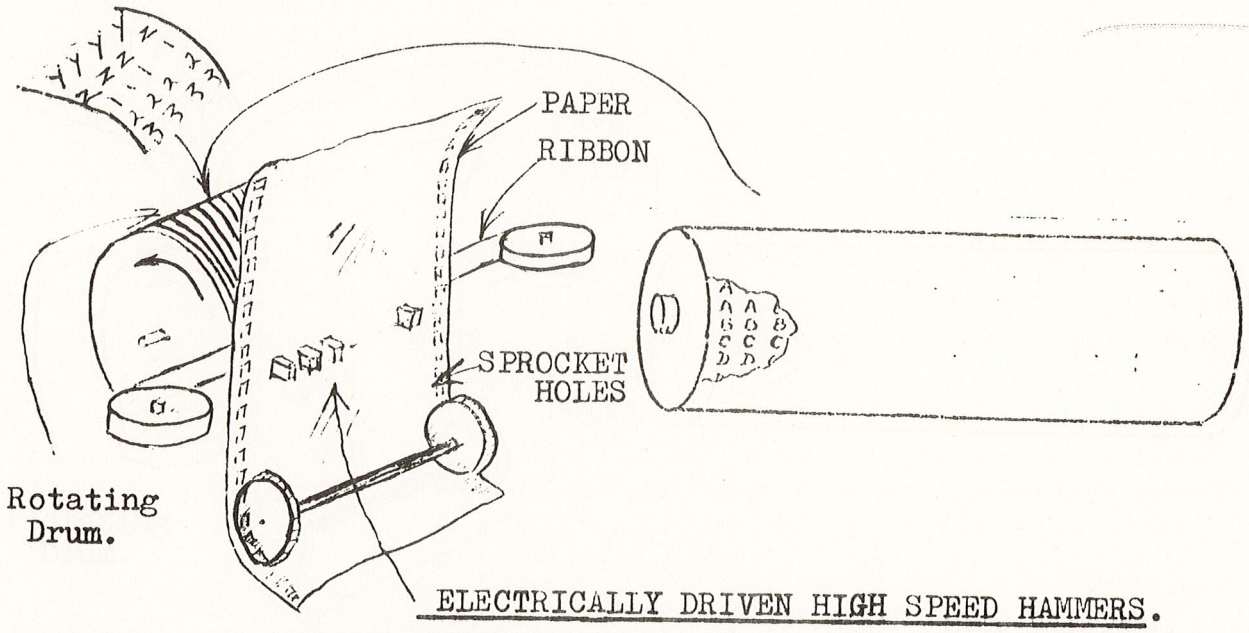
The belt may contain a number of sets of characters to cut down the time until the desired character lines up under the hammer. Printers now available can operate at speeds over 2000 lines per minute.

Synchronising the operation is important because there is not a single hammer stroke and paper feed operation. Each hammer strikes as the correct character passes under the head. After all hammers have struck once, the paper feed advances one line and the operation repeats. Although these speeds are seemingly very fast, data is being generated hundreds of times faster in the computer.

One device that uses this principle is the Terminett 300 which will be used on ARE 11 exchanges.

Rotating Drum Printer (or Drum on the fly)

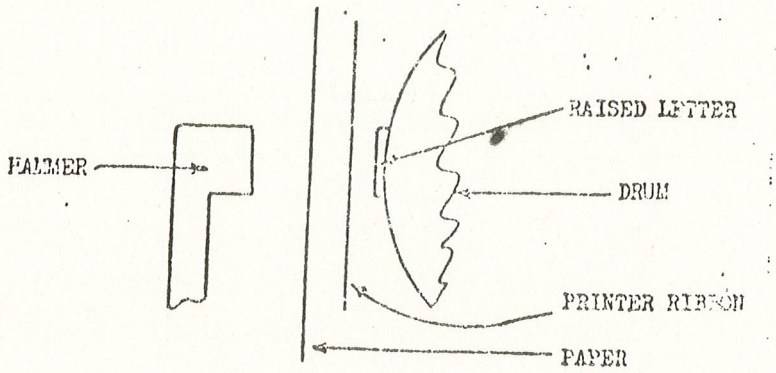
This form of printer uses a drum which with each character appearing around the drum in each printing position. The drum may have between 120 - 144 characters per line.



ELECTRICALLY DRIVEN HIGH SPEED HAMMERS.

ROTATING DRUM PRINTER.

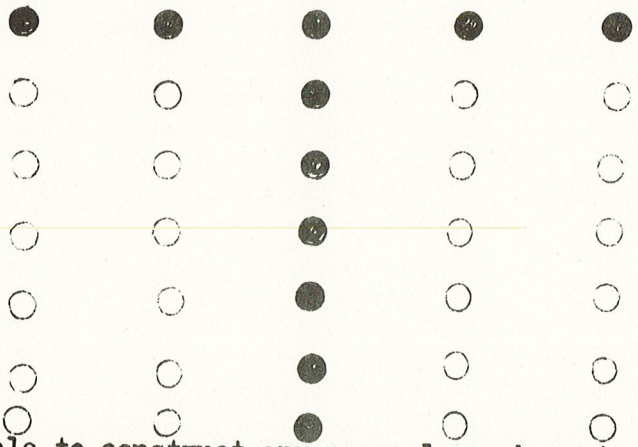
Commands for all characters of a line are fed to the printer at one time. As each line of the drum passes by the fixed hammer the individual hammers strike. For example if the letter "A" was in position all the "A"'s in the line will be printed then all "B's" etc. It is possible to produce a complete line of print in one revolution of the drum. Printers of this type operate at speeds of between 200 - 1200 lines per minute. They can provide up to 64 characters for up to 144 printing positions per line.



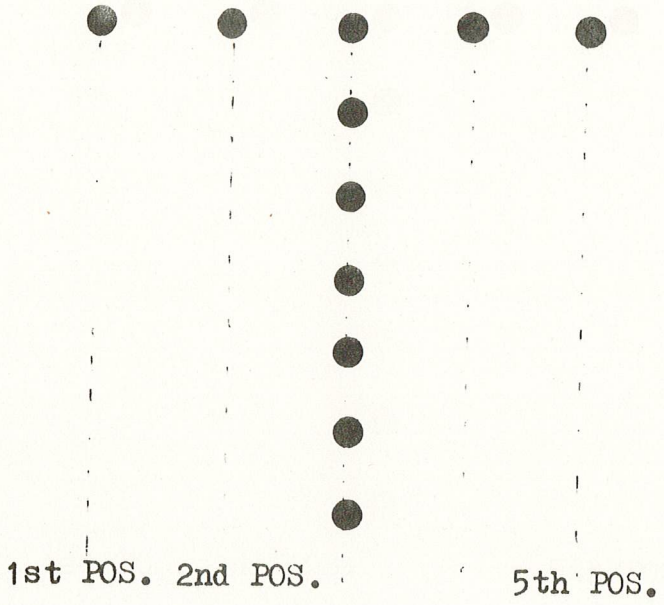
Matrix Printer (Sargum)

This type of printer uses a 5 x 7 matrix of dots to assemble the characters. It is microprocessor controlled and uses a set of six stepping motors to control carriage movements and paper feed as well as the printing mechanism.

The characters are constructed from a 5 x 7 data matrix (see below). From this:



matrix it is possible to construct any numeral or character. The printer head itself is a row of seven punches with seven hammers attached as a unit. To print the first character of a line the printing head is stepped into position and part of the character is printed. The head is then stepped to second position and the second part is printed e.g. for the letter T the following steps would occur.



CONSTRUCTION OF THE LETTER "T"

5x7 MATRIX

VISUAL DISPLAY UNIT (V.D.U.)

A device that is gaining importance as an output unit of a computer is the visual display unit. A typical unit incorporates a typewriter input keyboard and a C.R.T. output display. Data is entered on the keyboard as on a computer typewriter and electrical signals are generated for transmission to the computer. The computer generated binary data is then fed back to the C.R.T. unit as electrical signals to be displayed visually. The fast printing speed of the C.R.T. unit allows for quick display of a file or record of information. Bank transactions and airline reservation systems are two examples of V.D.U. display applications. The desired information displayed can be modified via the keyboard and new data stored back in the computer records. When "hard" copy is desired some systems employed microfilm or other reproducing devices to be operated by the computer.

V.D.U. may include storage facility (Core or I.C. Storage Units) with capacity of say 1024 characters. Displayed data is held in the V.D.U. storage section so that the computer need not be involved in the display presentation unless new data is transmitted. The stored data is then repeatedly swept across the C.R.T. screen as the picture on a home TV is scanned. Refresh rates of 60Hz are common - meaning that the full display is repeatedly written on the C.R.T., about 60 times per second so that, it appears steady. Transmission of data to and from the V.D.U. may be rated in Bauds.

V.D.U.'s used in the TELNET system transmit and receive at 4800 ~~Bauds~~. BITS PER SEC

A V.D.U. may also have magnetic tape cassette input/output capability to provide easy entry or storage of displayed data. Other options may include hard copy from an electrostatic copier or teleprinter.